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The breakdown voltage in GaAs field effect transistors (FET) has been the fundamental limitation of power performance in these devices. Previous studies have identified the high electric field at the drain edge of the gate metal as the cause of breakdown. At the start of this project, we successfully demonstrated that a low-temperature-grown GaAs (LTG-GaAs) suface 'insulator' dramatically improved the breakdown voltage in a GaAs MISFET. Subsequent device studies have concentrated on the use of LTG-GaAs as a surface passivation layer in GaAs MESFETs due to the potential shortcomings of a MISFET in its rf performance. Despite the early success, very little was known about the relevant electrical properties of LTG-GaAs. To better understand why LTG-GaAs works, what are its device limitations, and how device performance can be further improved, an extensive study of the material properties of LTG-GaAs has been carried out in parallel with device fabrication and testing. In this report, the results from our investigations will be split into two sections. The first section will discuss issues related to the fundamental understanding of LTG-GaAs, the second with device results using LTG-GaAs surface layers.

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FINAL REPORT

PROJECT # AFOSR-91-0111

THE IMPACT OF LOW-TEMPERATURE MATERIALS ON THE BREAKDOWN AND NOISE PROPERTIES OF GaAs AND InP BASED HEMT'S AND FET'S

by

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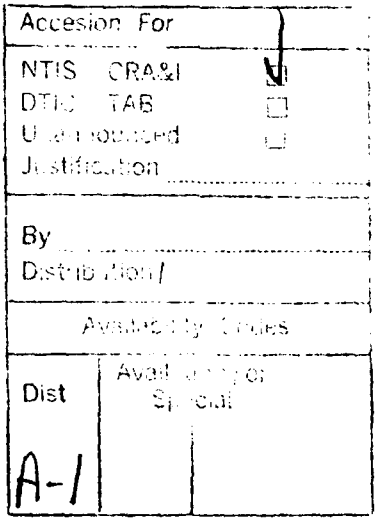
INTRODUCTION

The breakdown voltage in GaAs field effect transistors (FET) has been the fundamental limitation of power performance in these devices. Previous studies have identified the high electric field at the drain edge of the gate metal as the cause of breakdown. At the start of this project, we successfully demonstrated that a low-temperature-grown GaAs (LTG-GaAs) suface 'insulator' dramatically improved the breakdown voltage in a GaAs MISFET. Subsequent device studies have concentrated on the use of LTG-GaAs as a surface passivation layer in GaAs MESFETs due to the potential shortcomings of a MISFET in its rf performance. Despite the early success, very little was known about the relevant electrical properties of LTG-GaAs. To better understand why LTG-GaAs works, what are its device limitations, and how device performance can be further improved, an extensive study of the material properties of LTG-GaAs has been carried out in parallel with device fabrication and testing. In this report, the results from our investigations will be split into two sections. The first section will discuss issues related to the fundamental understanding of LTG-GaAs, the second with device results using LTG-GaAs surface layers.



SE( )N I - Material Characterization of LTG-GaAs

Low-Field Electronic properties

The fundamental material characteristic of GaAs grown by molecular beam epitaxy (MBE) at low temperature is its non-stoichiometry. For growth at substrate temperatures below ~300°C the as-grown epilayer is highly As rich (up to ~2% excess As). As a result, the electronic properties of LTG-GaAs are dominated by the large number of native defects present (in various guises). In addition, the defect populations change dramatically with thermal treatments, which in turn alters the electronic properties. This is illustrated in Fig. 1 which shows the effect of anneal temperature on the conductivity of a 1μm thick layer of LTG-GaAs grown at 250°C. Astonishingly, the room temperature conductivity changes by ~5 orders of magnitude; from a conductivity of 10^{-4} S/cm as-grown to a highly resitive 10^{-9} S/cm following an anneal at 650°C or higher.

When the temperature dependence of the low field current through a LTG-GaAs layer is examined, we find that the activation energy near room temperature also changes dramatically with anneal temperature (Fig. 2). In totality, our results suggest the following scenario. For as-grown material and following anneals up to 450°C, low-field transport is due to hopping through a defect band situated 0.3-0.4eV below the conduction band edge. The uncertainty in the energy comes from the difficulty in measuring directly the Fermi level in this material. For anneal temperatures above 500°C hopping takes place through a second defect band situated 0.6-0.7 eV below the conduction band edge. Direct measurement of the defect energy level in this case is relatively simple (slightly above room temperature band conduction starts to dominate), so the range in the activation energy in this case probably reflects the changing defect bandwidth as the defect concentrations change. As the anneal temperature is increased defects anneal out, which leads to a decrease in the hopping transport. Following an anneal at 600°C the small number of electrons in the conduction band start to dominate the room temperature transport. This is summarized schematically in Fig 3.

Our evidence for two distinct defect levels (~0.35 eV and ~0.65eV) is shown in Fig. 4. In this figure, the carrier sheet concentration in a 1250Å thick p-GaAs layer grown with an AlAs/LTG-GaAs cap is plotted as a function of anneal temperature. The Fermi-level in the LTG-GaAs cap is pinned close to the dominant defect level due to the high density of traps. As the Fermi-level in the cap changes so does the channel depletion width, which is easily measured using

the Hall effect. Between 400°C and 500°C we observe a sudden decrease in the depletion width . The decrease is in good agreement with the expected change from E_F-E_C~0.35eV to E_F-E_C~0.65eV in the LTG-GaAs cap corresponding to different dominant defects.

Figure 4 also shows the effectiveness of a 100Å AlAs layer as a diffusion barrier in preventing the excess As in the cap from backdiffusing. By selectively etching off the LTG-GaAs cap and AlAs after an anneal, the channel depletion width depends only on the net acceptor concentration in the channel. We observe this to be constant for anneals as high as 700°C, meaning no deep donors backdiffuse and compensate the channel acceptors. Without the AlAs layer significant compensation is observed (not shown). The use of a diffusion barrier is essential to the successful implementation of LTG-GaAs surface layers in GaAs MESFET's.

High field transport modeling

Since LTG-GaAs is a poor conductor, its device applications invariably involve high electric fields. This is certainly true for its use as a surface layer under or near the gate metal in GaAs MESFETs. Therefore it is desireable to measure and model the high field transport in this material. As discussed above, there are two regimes corresponding to hopping conduction and band conduction. We examined the band conduction regime first since we are primarily interested in using the high resistivity LTG-GaAs obtained following high temperature anneals.

LTG-GaAs annealed at temperatures higher than 550°C contains large (20Å-200Å diameter depending on anneal temperature) arsenic precipitates buried in a GaAs matrix. Figure 5 shows a cross-section transmission electron micrograph of the precipitates. This fact led others to propose a "buried Schottky barrier" model to explain the high resistivity of the annealed material. In this model, As precipitates pin the Fermi-level near midgap in much the same way that a metal on GaAs forms a Schottky contact with a barrier height ~0.7eV. By extension, we propose that under high electric fields the current transport in LTG-GaAs should be limited by the emission of electrons from these buried metal spheres. A simple one-dimensional model that considers LTG-GaAs as a series of back-to-back Schottky diodes yields good quantitative agreement with the experimental data, as shown in Fig. 6. Our simple model shows that the high field transport is due to the field-assisted tunneling emission of electrons from the As precipitates into the conduction band.

We have only recently turned our attention to hopping conduction behavior in high electric fields. Preliminary results suggest that the field dependence of the conductivity is in agreement with existing theories developed for hopping conduction in shallow impurity bands. We observe a $\ln \sigma \sim E$ dependence, which is due to the electric field lowering of the energy required to make a hop along the direction of the field (Fig 7.). This work is continuing.

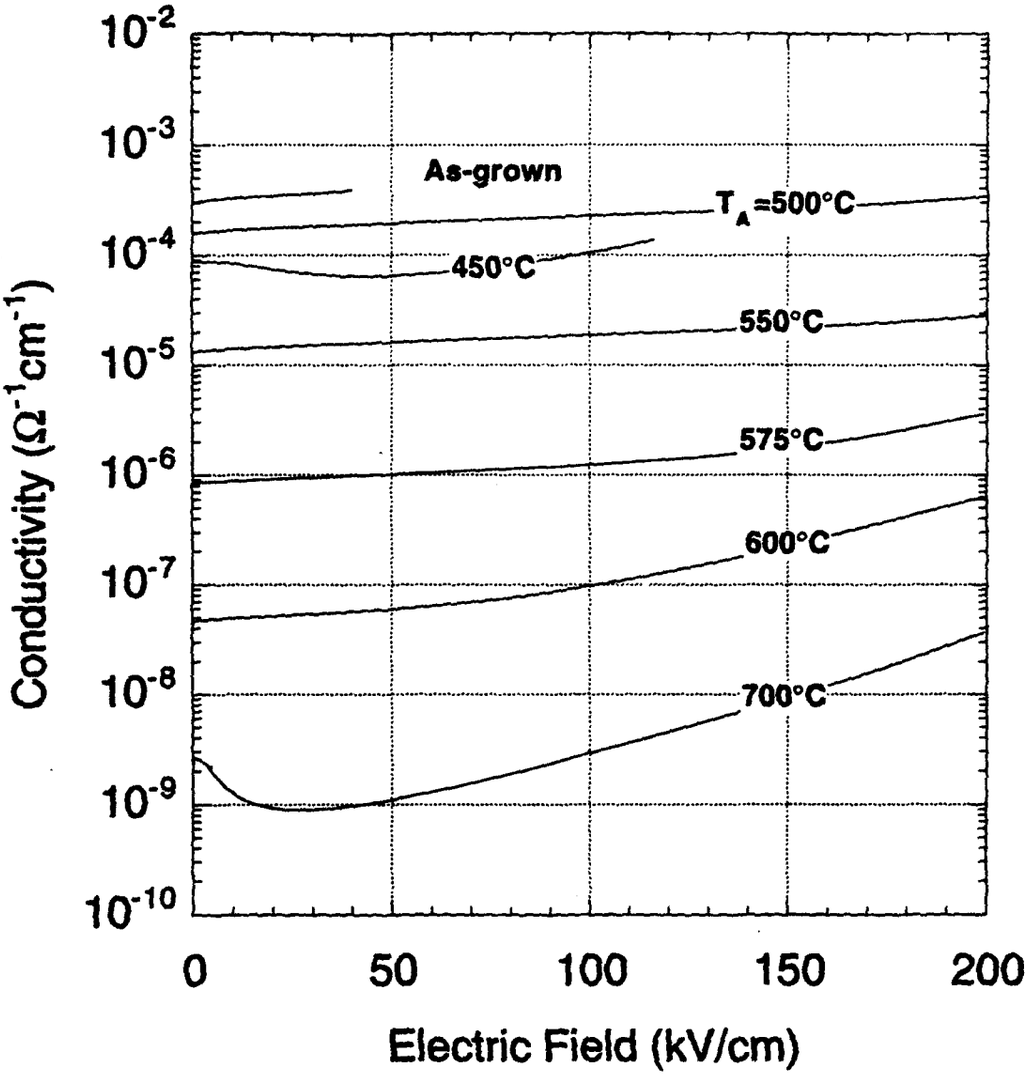


Figure 1. LTG-GaAs room temperature conductivity vs electric field for different anneal temperatures. 1μm thick layer was grown at 250°C

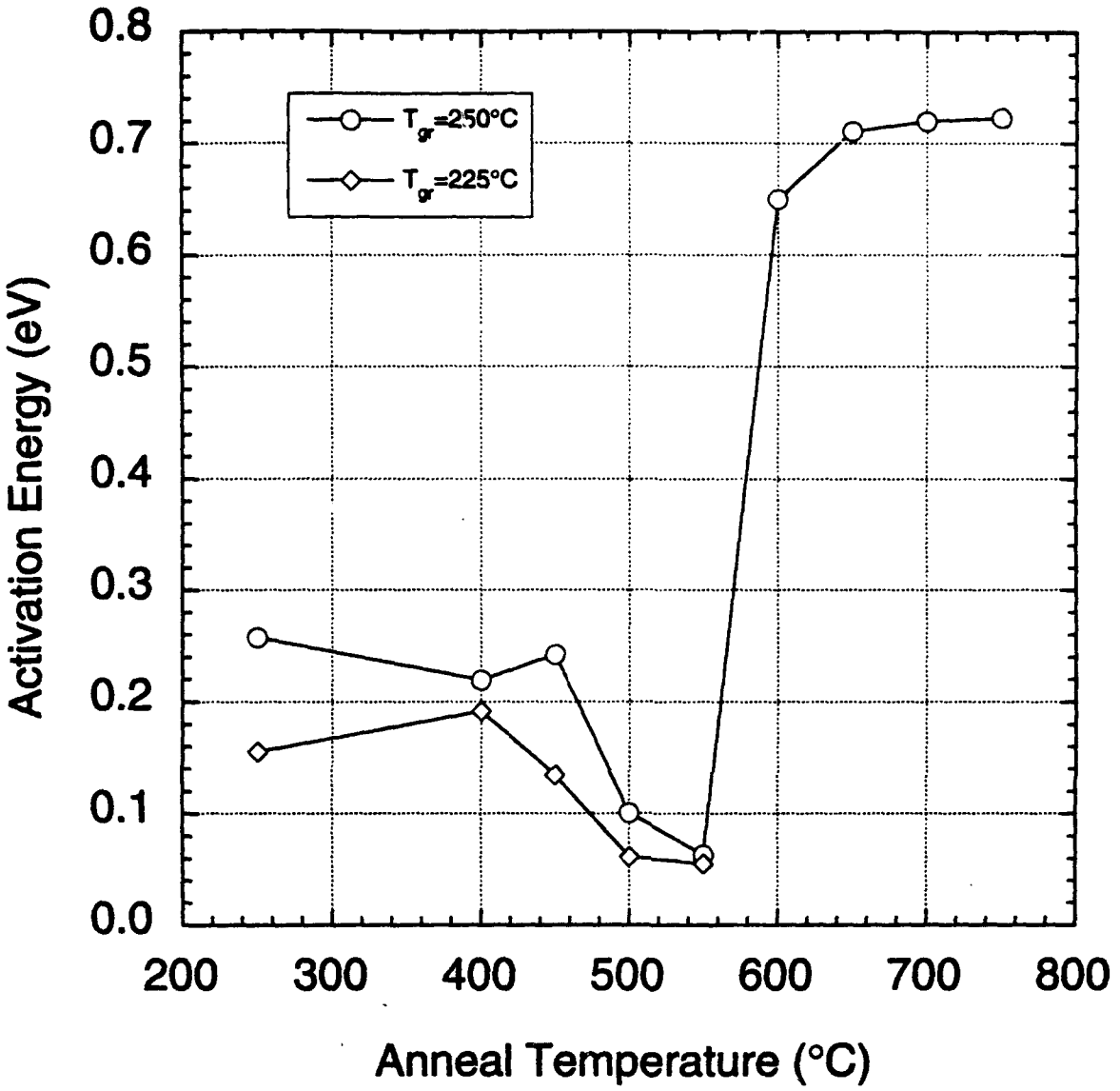
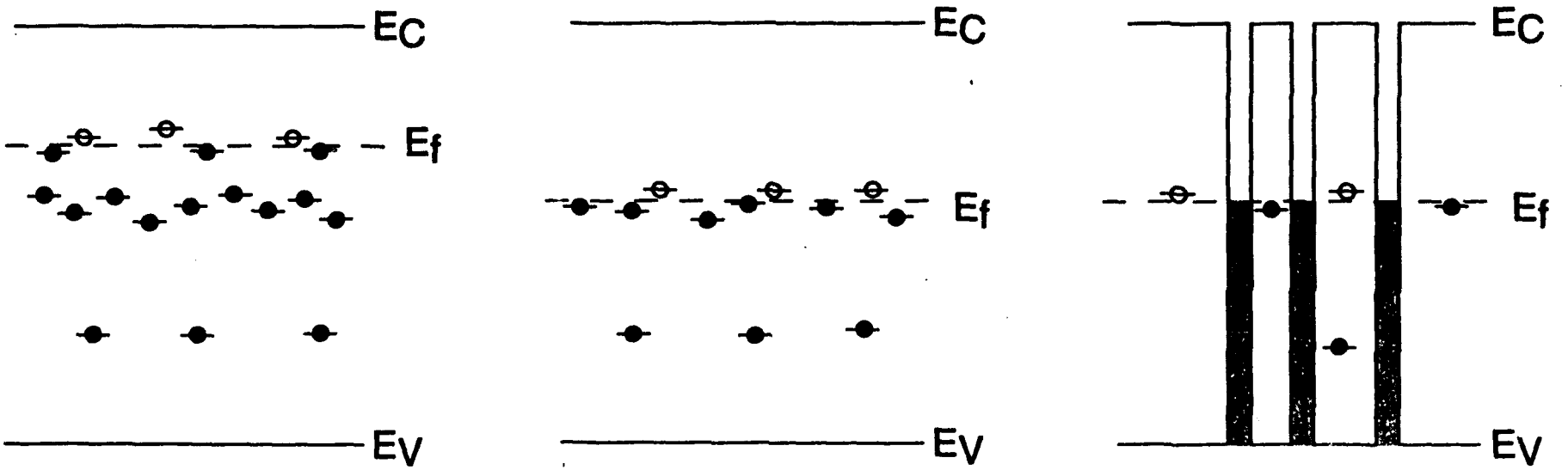


Figure 2. Activation energy of LTG-GaAs conductivity near room temperature as a function of the sample anneal temperature. The sudden increase at 600°C shows the transition from hopping conduction to free carrier conduction

Figure 3. Schematic showing relevant band diagram of LTG-GaAs for different annealing conditions



T_A=450°C
E_f-E_C~0.3 eV
band conduction

T_A=500°C to 600°C
E_f-E_C~0.6 eV
hopping conduction

T_A=650°C to 800°C
E_f-E_C~0.6 eV
thermally-assisted tunneling
from metallic precipitates

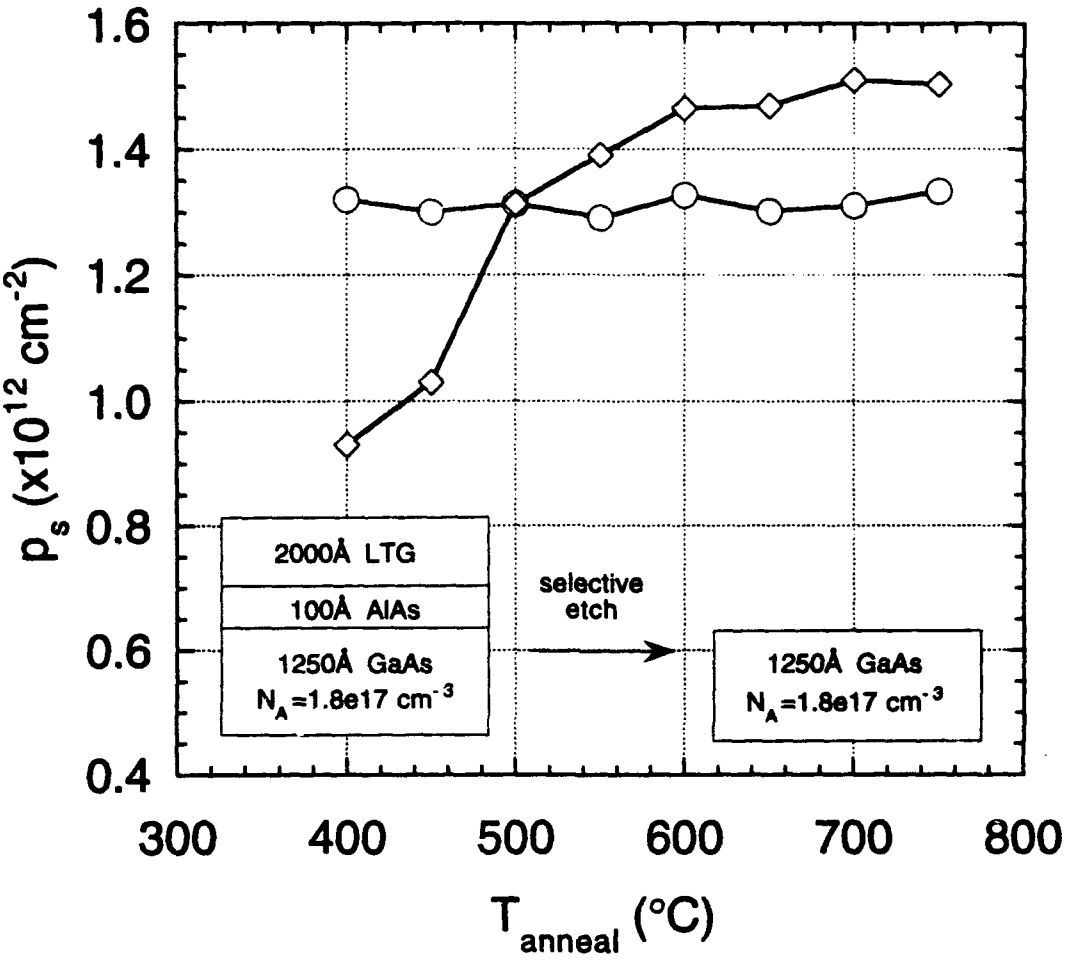


Figure 4. Effect of annealing temperature on hole sheet concentration in p-GaAs channel with LTG-GaAs cap and 100Å AlAs diffusion barrier.Open circles are for measurements with the LTG-GaAs cap etched off.

Figure 5. Cross section TEM showing As precipitates in LTG-GaAs layer following a high temperature anneal at ~650°C.

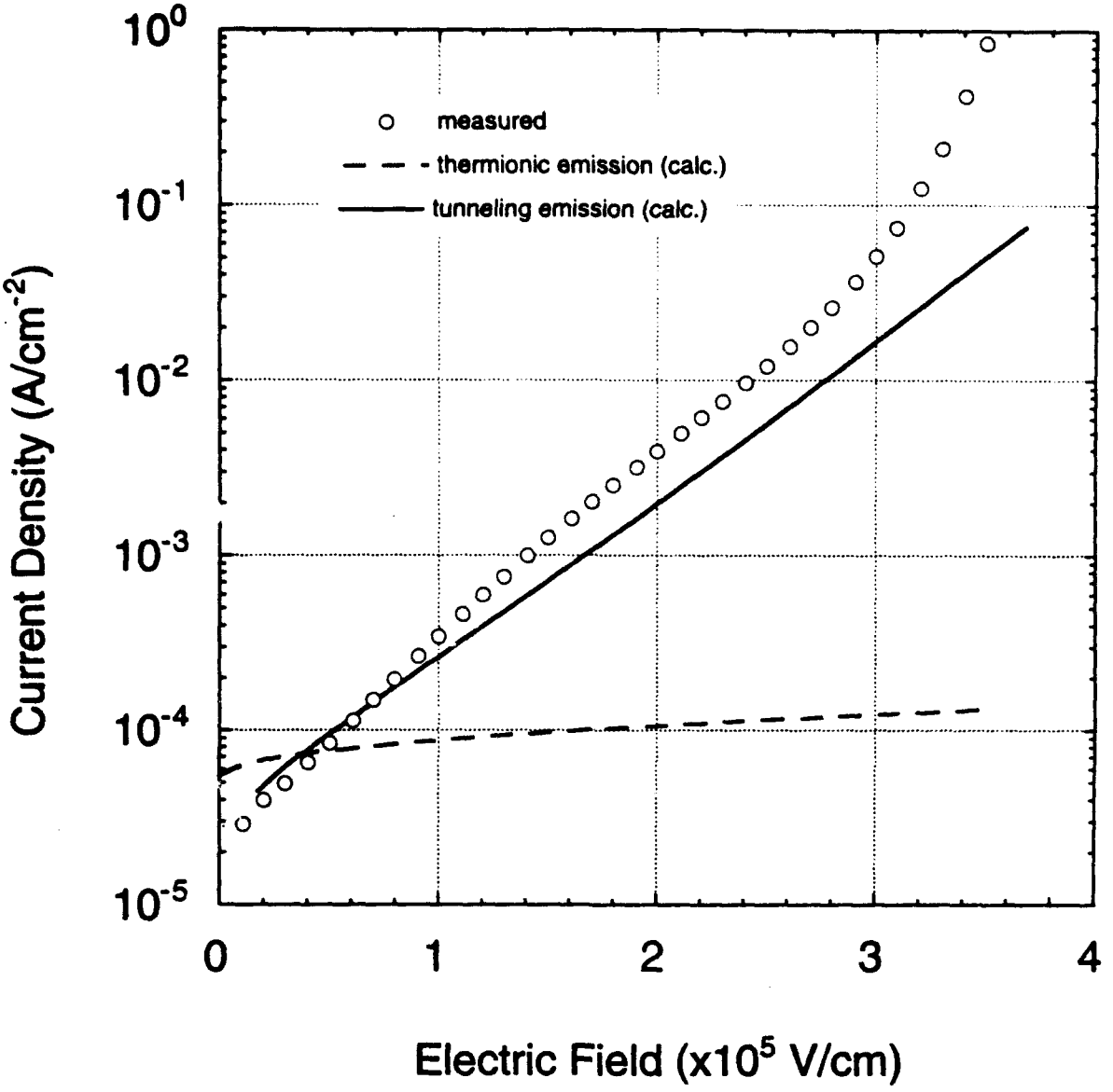


Figure 6. Room temperature high-field transport in LTG-GaAs annealed at 700°C. LTG-GaAs is modeled as a series of back-to-back Schottky diodes with transport limited by field-assisted tunneling emission from metallic As precipitates. There is good agreement between the calculated curve and the experimental data if a Schottky barrier height of 0.6eV is assumed.

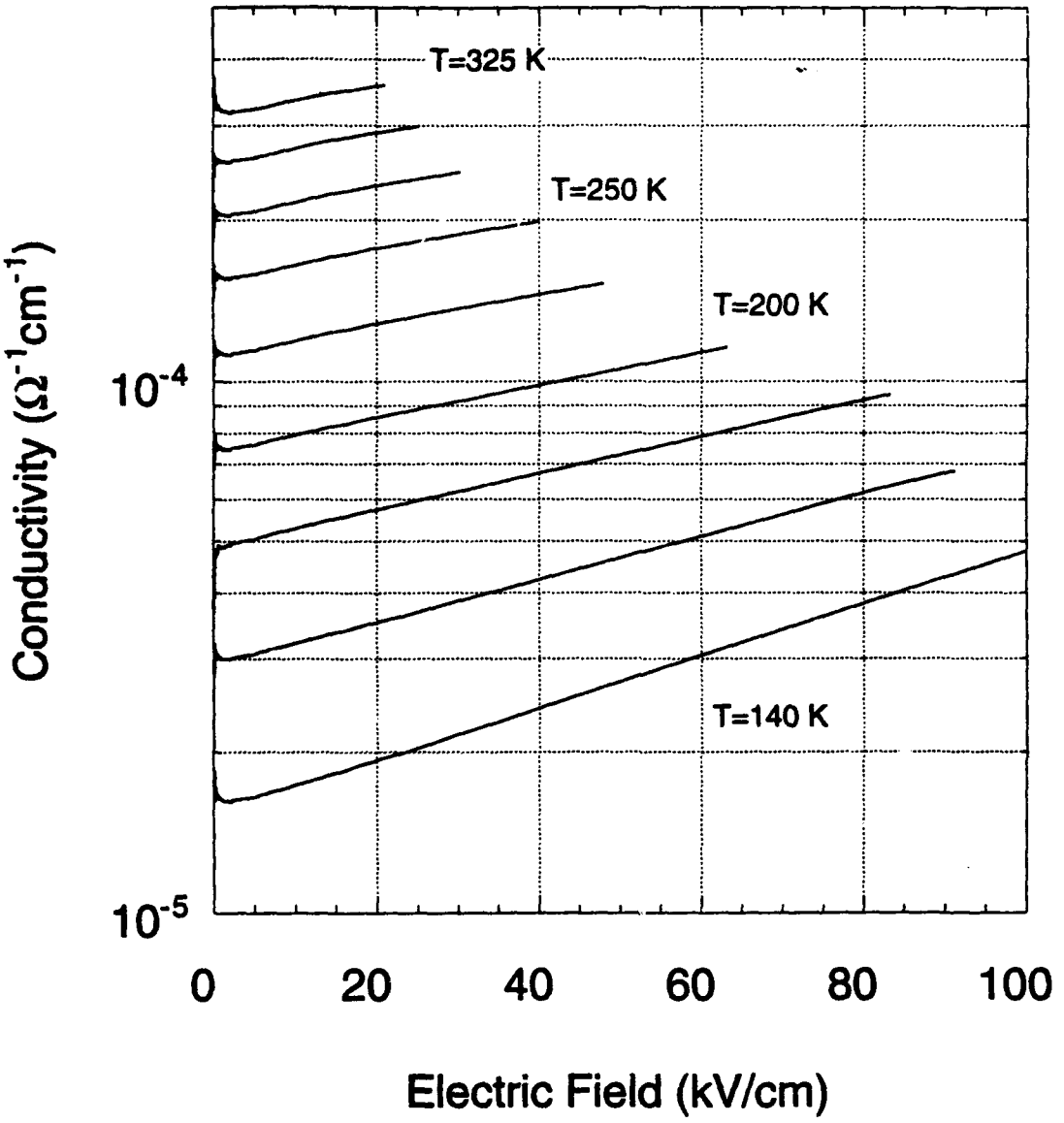


Figure 7. Measured conductivity versus applied electric field for a 1μm thick LTG-GaAs annealed at 500°C with temperature as a parameter. Conduction is due to hopping in a defect band ~0.65eV below the conduction band.

SECTION II - GaAs based Microwave MESFETs with LTG-GaAs passivation

The breakdown voltage in the field effect transistor (FET) has been the fundamental limitation of the power performance of the device. Previous works have identified the high electric field at the drain edge of the gate metal to be the main culprit that cause the breakdown in devices. At the start of the project, we have successfully demonstrated that Low-Temperature-Grown GaAs surface insulator can dramatically improve the breakdown voltage in GaAs MISFET. However, due to the potential shortcomings of MISFET in its rf performance (ie high dispersion of the tranconductance), we have concentrated our efforts mainly into LTG-GaAs passivation in MESFET. We have fabricated a device with LTG_6-GaAs (annealed at 600°C) passivation in which we obtained more than twice the power density from a conventional commercial devices. By investigating the gate-drain diode characteristics as a function of the temperature, we have gained an understanding into how LTG-GaAs can improve the power performance of the MESFETs. Recently, we have investigated the passivation of GaAs MESFET with LTG_4-GaAs (annealed at 400°C). The pinning of the fermi level of LTG_4-GaAs at about 0.3 eV from the bottom of the conduction band make it a potential ideal passivation layer for near-planar devices with reduced parasitic resistances.

In this section of the report, we will discuss the procedures and results from these investigation into two parts, the first part deals with LTG_6-GaAs passivation, and the second with LTG_4-GaAs passivation :

MESFETs with LTG$_6$-GaAs Passivation

The epitaxial structure and device cross-section is shown in Fig. 8. The growth temperature of the LTG GaAs and AlGaAs was 200°C and the anneal was carried out in-situ at 600°C. The mobility and sheet charge concentration were determined from Van der Pauw measurements to be 3700 $cm^2/V\text{-}s$ and $3.8x10^{12}$ cm^{-2} respectively. The fabrication process of the device began with the definition of the mesa by wet chemical etching of the patterned sample. Next, the source-drain regions were defined and reactive-ion-etching (RIE) with Cl_2 was used to remove the insulating layers and expose the channel. AuGe/Ni/Au ohmic contacts were defined by lift-off and subsequent rapid-thermal-annealing at 375°C for 15 seconds resulting in a contact resistance of 0.3 Ω-mm . The foot of the gate was then defined and again RIE with Cl_2 was used to etch away the LTG layers down to the channel. Finally, the overlapping gate mask was aligned to the defined gate foot print and the gate was then formed by lift-off of Ti/Au metals.

The temperature characteristics of the gate-drain diode of a GaAs MESFET with 1.2 μm gate length and LTG-AlGaAs/GaAs passivation is shown in Fig. 9a. At 300 K, the diode shows a high breakdown voltage of 34 V. However, as the temperature is lowered, the breakdown voltage first decreased monotonically, then saturated to about 10 V at 77 K. In comparison, Fig. 9b shows the temperature-dependence behavior of a gate-drain diode in a conventional GaAs MESFET ($N_d = 3 \times 10^{17}$ cm^{-3}). In the conventional device, the observed dependence of the breakdown voltage with temperature is very small.

The strong temperature dependence of the breakdown voltage observed in a MESFET with LTG-GaAs passivation can be explained by using existing breakdown models (++). In the low gate voltage range, the current-voltage characteristics shown in Fig. 10 agree with the transport model of thermionically assisted tunneling between precipitates proposed by Ibbetson *et al* . The electrons propagate from the gate metal onto the LTG-GaAs passivation layer by tunneling via the assistance of the local electric field and the temperature. However, since the electric field drops off rapidly away from the gate metal, the injected electrons are localized at those precipitates that are close to the gate metal. The resulting excess of the negative charges in the vicinity of the gate metal next to the drain would redistribute the associated electric field. Consequently the peak electric field at the edge of the gate is alleviated. As the temperature is lowered, the number of electrons that can thermionically field emit into the precipitates is significantly reduced, thus the LTG-GaAs becomes less effective in reducing the field. At low temperature (77 K), this field alleviation mechanism becomes relatively ineffective; thus the breakdown voltage saturates at that of a conventional GaAs MESFET. Figure 11 shows schematically the electric field distribution

with the field alleviation by the charged precipitates. The most conservative hypothesis we can draw is that, since the response of traps at low temperature is similar to their high frequency response, the rf breakdown may be close to the breakdown voltage at 77 K. Even so, a large benefit results as explained below.

To obtain the maximum output power from MESFETs, the devices are usually biased at half of the breakdown voltage thereby allowing the rf signal to swing from zero to the rf breakdown voltage (BV_{rf}). However, the static electric field at the gate edge for LTG-passivated devices is low even at a gate-drain bias as high as BV_{rf} ($BV_{rf} << BV_{dc}$). We therefore expect that a full rf swing of $2xBV_{rf}$ can be accomodated in these devices, doubling (at the minimum) the rf power from passivated devices compared to conventional GaAs MESFETs. The power measurements on our device shown in Fig. 12 supports the above hypothesis.

MESFETs with LTG_4-GaAs Passivation

The pinning of the surface Fermi level in GaAs has effected many devices's characteristics. In particular, the depletion regions in the gate-source and gate-drain regions in a MESFET from this surface pinning plays a major role in the parasitic resistances of the device. In order to compensate for this deleterious effect, many workers have applied an n+ cappin top of the device and then recess etch away the n+ capping underneath the gate. Howe ne recess technology gives rise to another problem, the uniformity of the threshold voltages across the sample. Furthermore, the required etch depth is relatively very deep, which makes it an incompatible technology for sub-micron gate lengths, and the n+ capping in these devices would dramatic degrade the breakdown voltage in the device. Thus an ideal passivation layer for parasitic resistances reduction would be a **thin layer** of some materials that would alleviate the fermi level pinning without compromising the breakdown voltage of the device. Low-Temperature-Grown GaAs annealed at 400°C (LTG_4) would be a potential candidate for such role.

From the studies of the material properties of LTG-GaAs, it has been observed that the bulk fermi level is pinned at about 0.3 eV from the conduction band with a trap density of $N_a \sim 10^{19}$ cm^{-3} and $N_d \sim 10^{19}$ cm^{-3}. Consequentially, the surface fermi level comes to that of the bulk within ~200 Å (depletion layer). However, since the charges in the LTG_4-GaAs are mainly trapped charges, the LTG_4-GaAs remains relatively insulating.We have fabricated a MESFET that has been passivated with a thin layer (500Å) of LTG_4-GaAs and one that was without the LTG_4-GaAs passivation (ie the capping is selectively etched off). The device characteristics are shown in Fig. 13 and Fig. 14. Comparing these two devices, we see that by passivating with LTG_4-GaAs, the device's extrinsic maximum current density and transconductance have improved; This indicates that the parasitic resistances have been reduced, while the breakdown voltage of the device did not suffer any setback. Currently, we are actively investigating and optimizing the parameters for the passivation layer of LTG_4-GaAs.

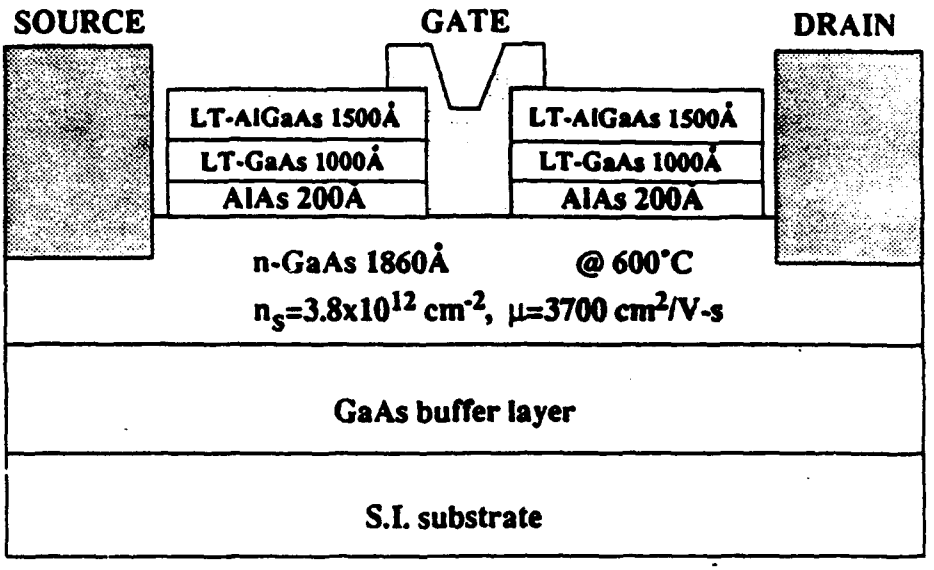
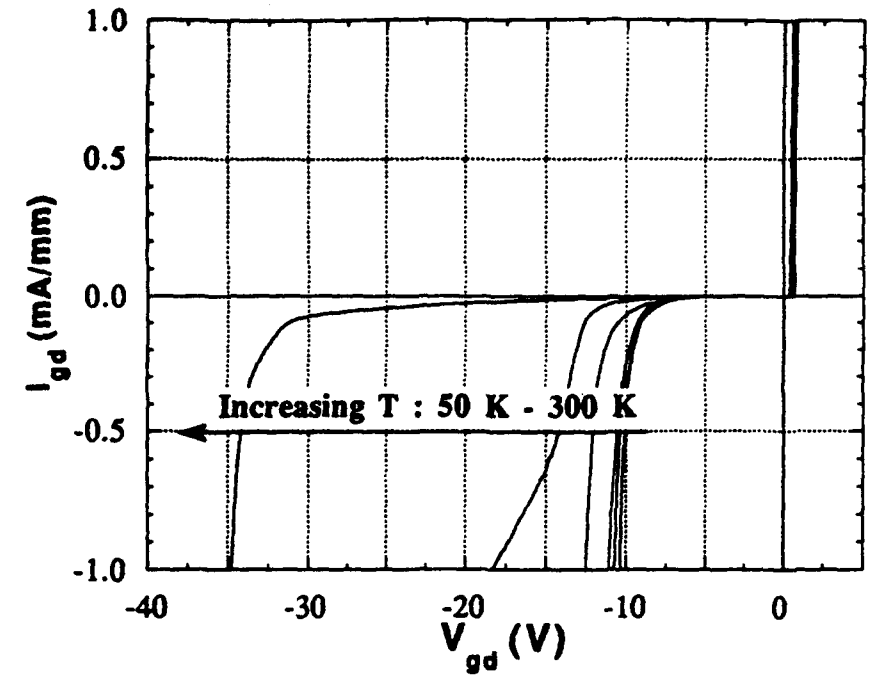


Figure 8. Epitaxial structure and device cross-section for MESFET with LTG-GaAs surface passivation layer.



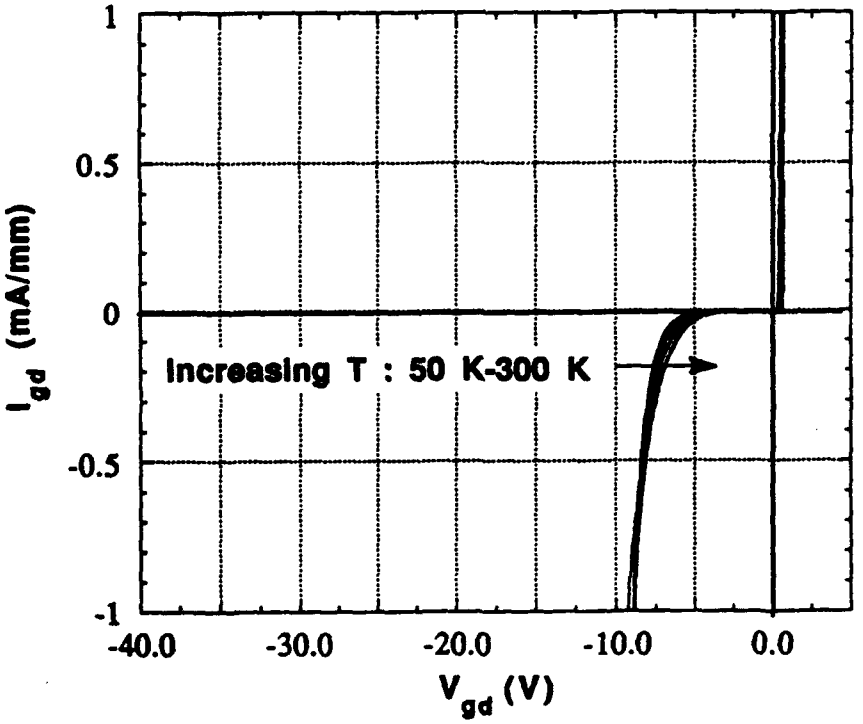


Figure 9.

(a) Temperature characteristics of the gate-drain diode in a GaAs MESFET with LTG-AlGaAs/GaAs passivation layer.

(b) Temperature characteristics of the gate-drain diode in a conventional GaAs MESFET.

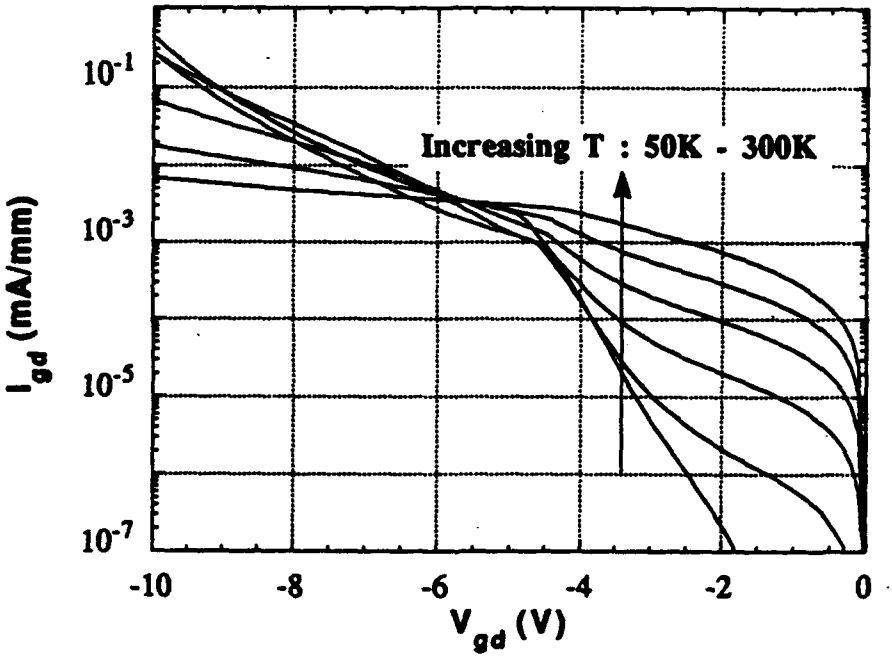


Figure 10. Gate-drain diode I-V characteristics for device in Fig. 9a shown on semilog plot. Data agrees well with transport measurements on bulk LTG-GaAs layers (see Fig. 6).

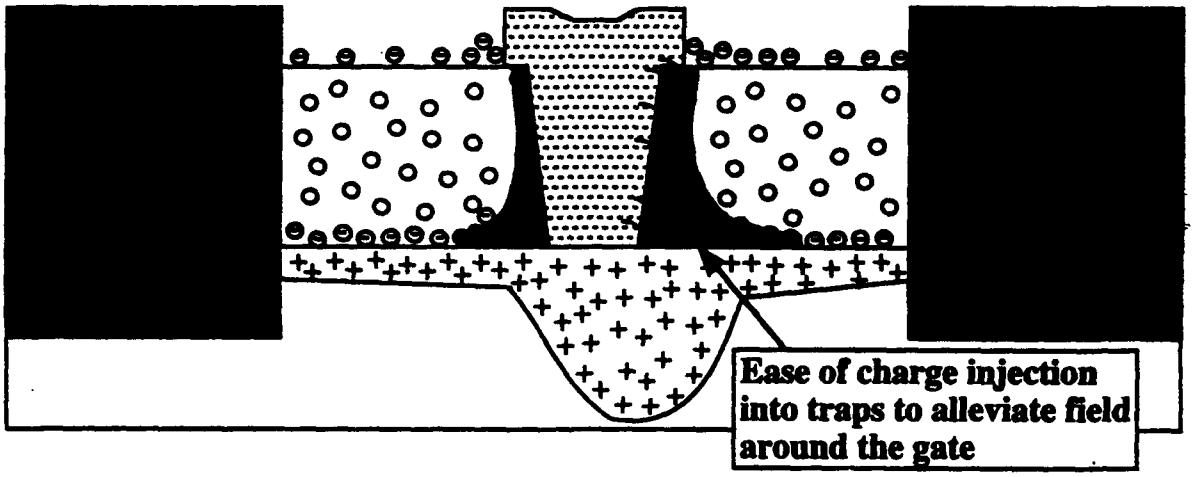


Figure 11. Schematic representation of the electric field distribution near MESFET gate metal with field alleviation due to charged precipitates.

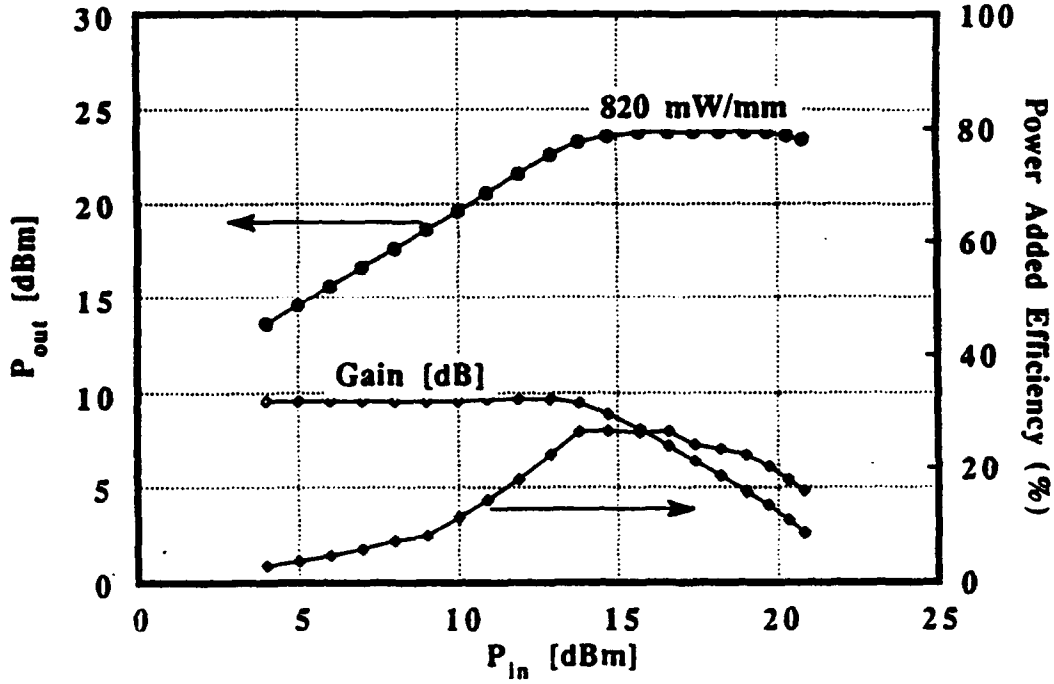


Figure 12. Power performance results for MESFET with LTG-GaAs surface passivation layer.

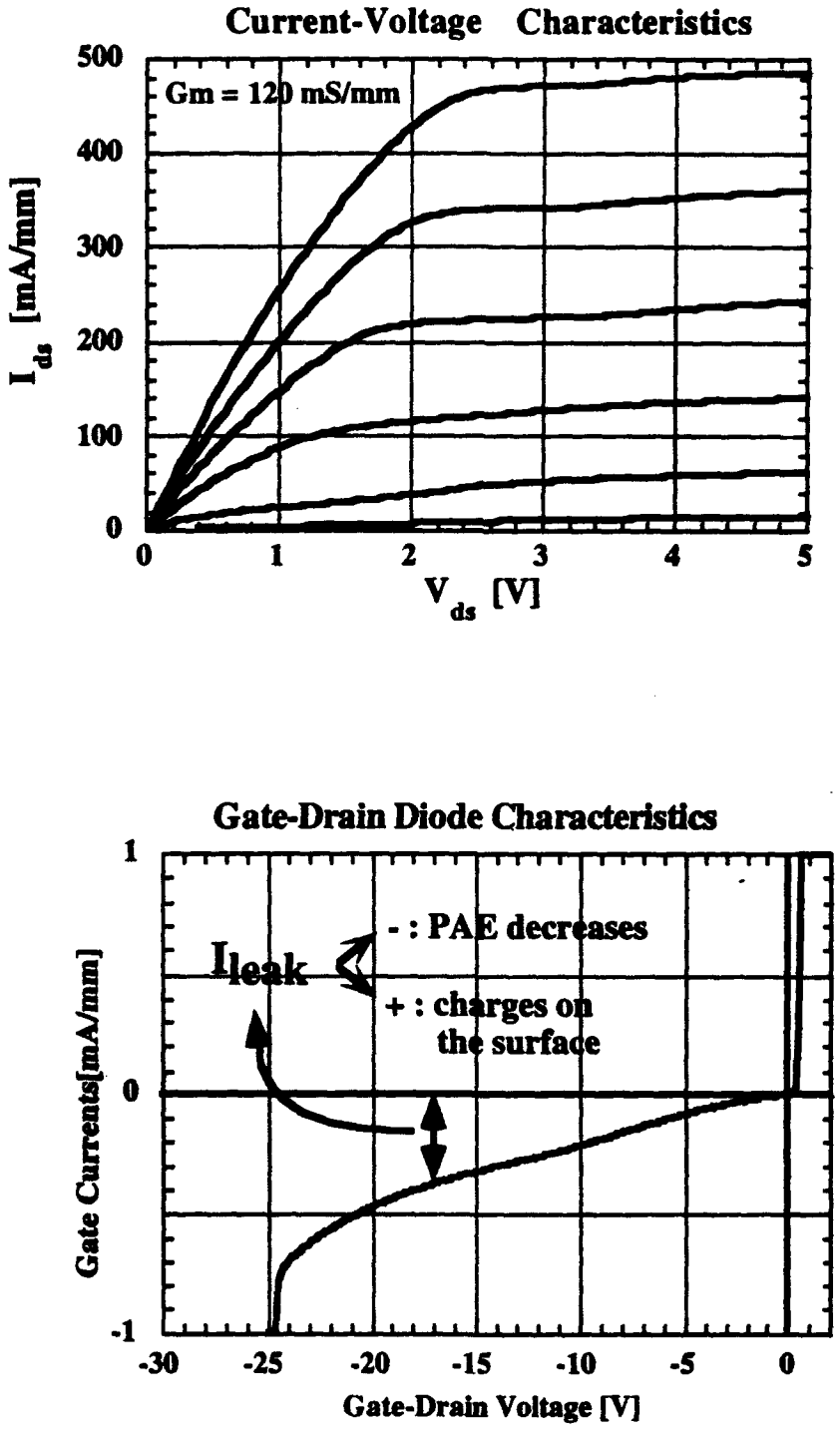
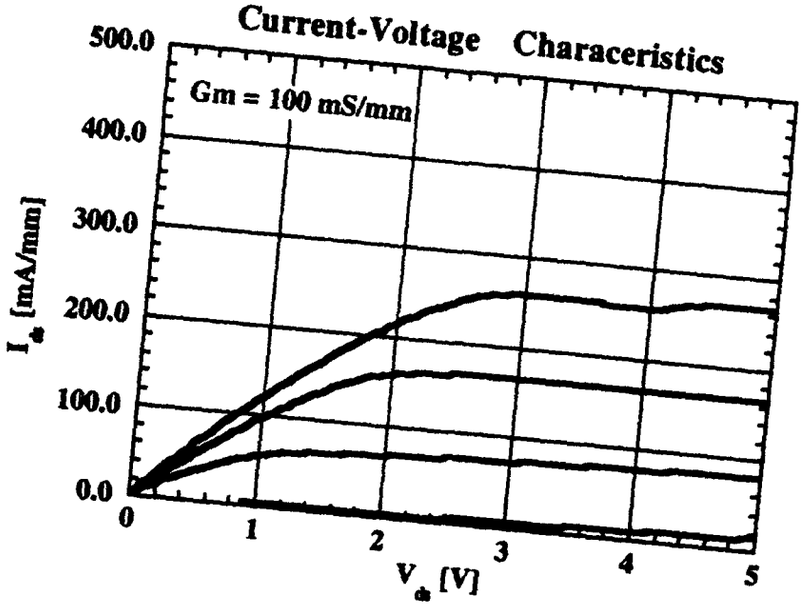


Figure 13. DC characteristics of MESFET with LTG-GaAs surface passivation layer which has been annealed at 400°C



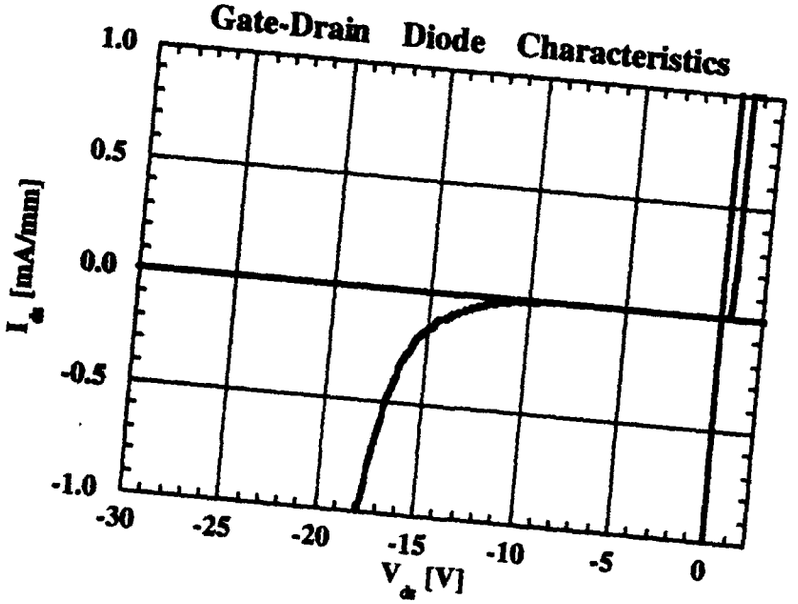


Figure 14. DC characteristics of MESFET with LTG-GaAs passivation layer etched off. Note reduction in Gm and Ids compared with device in Fig. 13.

Publication List

A list of publications supported by the contract is given below

Improved Breakdown Voltage in GaAs MESFET's Utilizing Surface Layers of GaAs Grown at a Low Temperature by MBE
L.-W. Yin, Y. Hwang, J. H. Lee, R. M. Kolbas, R. J. Trew, and U. K. Mishra, IEEE Electron Device Letters, vol. **11**, No. 12, December (1990).

Confinement of Excess Arsenic Incorporated in Thin Layers of MBE Grown Low-Temperature GaAs
J. P. Ibbetson, C. R. Bolognesi, H. Weman, A. C. Gossard, and U. K. Mishra, Proceedings of the 18th Int. Symp. on GaAs and Related Comp., Seattle, WA.

Investigation of the Electronic Properties of in-situ Annealed Low-Temperature Gallium Arsenide Grown by MBE
L.-W. Yin, Y. Hwang, J. P. Ibbetson, M. M. Hashemi, T. Zhang, R. M. Kolbas, A. C. Gossard, and U. K. Mishra, Applied Physics Letters, **60**(16), 2005-2007, (1992).

Study of Modulation in GaAs MISFETs with LT-GaAs as a Gate Insulator,
L.-W. Yin, J. Ibbetson, M. M. Hashemi, W. Jiang, S.-Y. Hu, A. C. Gossard, and U. K. Mishra, Proceedings of the MRS Fall Meeting (Symposium F), Vol. **241**, 181-186 (1992).

Study of Transport Through Low-Temperature GaAs Surface Insulator Layers
J. P. Ibbetson, L.-W. Yin, M. M. Hashemi, A. C. Gossard, and U. K. Mishra, Proceedings of the MRS Fall Meeting, Vol. **241**, 187-192 (1992).

Electronic & Optoelectronic Applications of Materials Grown at a Low Temperature by MBE,
U.K. Mishra, and R.M. Kolbas, Proceedings of the MRS Fall Meeting, Vol. **241**, 159-170 (1992).

Observation of Impurity Effects on the Nucleation of Arsenic Precipitates in GaAs Grown at Low Temperatures by MBE,
J.P. Ibbetson, J.S. Speck, A.C. Gossard, U.K. Mishra, Appl. Phys. Lett., **62**(2), 169-171, (1993).

Investigation of Gate-Drain Breakdown Characteristics of Power GaAs MESFET with LTG Passivation as a Function of the Temperature
L.-W. Yin, N. Nguyen, Y. Hwang, J. Ibbetson, R.M. Kolbas, A.C. Gossard, U.K. Mishra, accepted for publication in the Proceedings of the MRS Spring Meeting, San Francisco, CA.

The Output Conductance in GaAs Air-Gap MESFETs
N.Nguyen, K. Kiziloglu, J. Ibbetson, L.W. Yin, M. Hashemi, and U.Mishra, accepted for publication in Proceeding from IEEE 50th Annual Device Research Conference, (1992).

The Role of Microstructure in the Electrical Properties of LT-Grown GaAs,
J.P. Ibbetson, N. Nguyen, J.S. Speck, U.K Mishra, J. Electron. Mat., **22**(12), 1421 (1993)

Temperature Investigation of the Gate-Drain Diode of Power GaAs MESFET with Low-Temperature-Grown (Al)GaAs Passivation
L.W. Yin, N.X. Nguyen, J.P. Ibbetson, R.M. Kolbas, A.C. Gossard, and U.K. Mishra, J. Electron. Mat., **22**(12), (1993)

Device Performance of Submicron MESFETS with LTG Pass-ivation
L.W. Yin, N.X. Nguyen, K. Kiziloglu, A.C. Gossard, and U.K. Mishra, accepted for publication in Proceedings of 1993 IEEE 14th Biennial Cornell Conference, August, 1993.

Observation of arsenic precipitates in GaInAs grown at low temperature on InP
J.P. Ibbetson, J.S. Speck, A.C. Gossard, and U.K. Mishra, Applied Physic Letters, 62(18), 2209 (1993).

Effects of As_4 flux on RHEED oscillations during growth of GaAs at low temperatures
J.P. Ibbetson, R.P. Mirin, U.K. Mishra, A.C. Gossard, J. Vac. Sci Tech. B, 12(2), 1050 (1994)

Appendix

Attached are selected reprints of journal articles sponsored by the contract AFOSR 91-0111

Inst. Phys. Conf. Ser. No 120: Chapter 2
Paper presented at Int. Symp. GaAs and Related Compounds, Seattle, 1991

Confinement of excess arsenic incorporated in thin layers of MBE-grown low-temperature GaAs

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Introduction

GaAs epilayers grown at low substrate temperatures (200-250°C) under otherwise normal MBE growth conditions are currently attracting much interest due to their unique electrical properties. Initially developed as buffer layers for power FET applications[1], Low-Temperature GaAs (LTGaAs) can reduce backgating in MESFETs [1]. Subsequently, surface layers of LTGaAs have also been employed to significantly improve MESFET gate-to-drain breakdown characteristics [2]. Most recently, indications of low-temperature (10K) superconductivity has also been reported in bulk LTGaAs [3], although this remains a controversial topic.

Material characterization studies have shown that the low growth temperature results in highly non-stoichiometric crystalline growth, with roughly 1 at.% excess As [4]. During annealing and/or postgrowth high temperature treatment the excess As redistributes itself in the crystal. In some cases metallic As precipitates have been observed [5].

Preventing out-diffusion of As-related defects into nearby active regions is very important for present and future applications of LTGaAs. Optical studies indicate that the presence of a LTGaAs buffer layer can significantly affect the quality of quantum wells ~1000Å away [6]. However, AlAs layers grown at normal growth temperatures (600°C) have been shown to prevent compensation of an n-type channel beneath LTGaAs surface layers [2]. In the present paper we present results on the optical properties of single and multiple quantum well structures incorporating thin layers (<150Å) of LTGaAs within barriers and well regions respectively. Photoluminescence (PL) is used to probe the quality of layers and interfaces in the immediate vicinity (~200Å) of LTGaAs layers,the optical properties of LTGaAs QW's, and the effectiveness of AlAs defect diffusion barriers.

MBE Growth

All samples in this study were grown in a Varian GENII solid source MBE system. Complete growth details will be published elsewhere [7]. All low-temperature (LT) growth was at a substrate temperature (T_{sub}) of 230°C as measured by a thermocouple. Otherwise growth occurred at T_{sub}=600°C.The growth rate was 0.5μm/hr, with an As_4:Ga beam equivalent pressure of 15:1.

Results

Two series of samples were grown. In the first series, a GaAs/AlGaAs single quantum well structure containing very thin layers of LTGaAs was studied. Bulk layers of LTGaAs have been shown to be optically dead, due to the large number of recombination centres they contain. In this study, the effect of these traps on the optical properties of thin layers of LTGaAs is determined. In sample A, 15Å of LTGaAs was inserted in the centre of a 150Å GaAs well. The growth was interrupted during the well growth to ramp down the temperature as described above. In sample B, just 3 monolayers of LTGaAs sandwiched by 4 monolayer thick confining barriers of AlAs grown at 600°C was inserted in the well. The structures are shown schematically in figure 1.

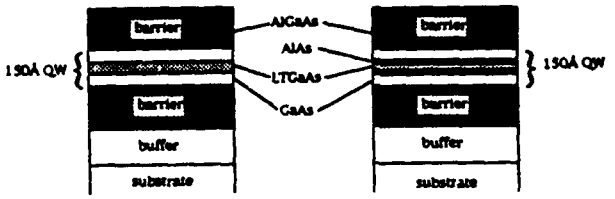

Figure 1

Schematic structure of samples A and B. The QW contains thin layers of LTGaAs. Sample B also has AlAs diffusion barriers. No PL was observed for either sample

Neither sample was specifically annealed after the LTGaAs layer was deposited, but growth of the upper barrier and completion of the structure means that both samples saw 600°C temperatures for 5 mins. No PL due to the well was observed in either sample, indicating that the density of non-radiative traps associated with these thin LTGaAs layers is sufficient to quench any detectable amount of radiative recombination. Since 1 at.% excess As translates into an enormously high defect density (~$1x10^{20}$ cm^{-3}) this may not be surprising. Yet, one might expect the defects to anneal out from such a thin LT layer as T_{sub} is raised. Obviously, this is not the case. Sample C contains no LTGaAs but was grown with a long growth interruption. It shows an intrinsic QW PL, confirming that unintentional impurity incorporation is not responsible for the PL quench.

The null result of samples A and B suggests that PL can be used to monitor the degree of As confinement by optically probing wells of unequal width surrounding a LTGaAs layer. This is the basis for the second series of growths and the results of samples D-H proved to be more interesting. The primary structure consists of three decoupled GaAs wells separated by 200Å thick barrier regions, as shown in figure 2. The first well to be grown is 150Å wide, followed by a 100Å well, and a 50Å well nearest to the surface. The upper and lower AlGaAs barriers are 500Å thick.

Sample H is a control sample. In this growth all three wells are grown at 600°C. There was no temperature ramping and no extended growth

interruptions. For samples D,E,F,G the 100Å well is grown at 230°C. In samples D and F, 30Å of AlAs is inserted in the 200Å thick barriers on either side of the LTGaAs layer in order to confine excess As. Samples D and E are annealed for 20 mins. at 600°C immediately following the central well in an As_4 flux of 5×10^{-6} torr, before proceeding with the remainder of the growth. Therefore significant redistribution of the LT-related defects is expected in these samples prior to the growth of the 50Å well. There is no anneal after the LTGaAs well in sample F or sample G. However, the remaining growth time for both samples is approximately 6 mins. at 600°C.

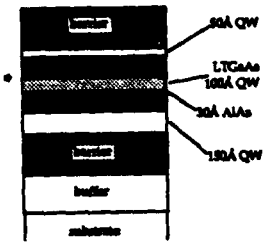

Figure 2

Growth structure for samples D-H. Three decoupled QW's, 50Å,100Å and 150Å wide. The middle (100Å) well is LTGaAs except in the control sample, H. Samples D and E are annealed for 20 mins. at 600°C following the 100Å well (*). The control barrier material in samples E and G does not include AlAs defect diffusion barriers.

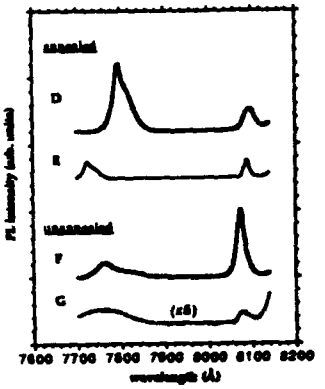

Figure 3

PL spectrum for samples D-G. D and E were annealed following the LTGaAs layer. D and F include AlAs diffusion barriers. Curves have been shifted vertically for clarity. The vertical scale has exaggerated by x5 for sample G.

The PL spectra corresponding to the four samples containing LTGaAs are shown in figure 3. Some PL due to the 150Å and 50Å wells are observed in all four samples. As expected, in no case do we detect PL due to the 100Å LTGaAs well itself. It is readily apparent that the presence of the LTGaAs layer has a significant effect on the quality of epilayers nearby.

The 50Å well double peak (due to monolayer fluctuations in the well-width) has broadened significantly in the unannealed samples which strongly suggests a degradation in the AlGaAs/GaAs interface quality. The optical efficiency of this well has also decreased compared to the annealed samples and the control sample, which suggests the introduction of non-radiative recombination centers in the well. These effects become increasingly large in sample G. In fact, the vertical scale has been exaggerated (x5) for sample G, and for this sample the peak is extremely broad (20 meV) and almost at the limit of detectability. In addition, there is a small (5-8 meV) shift in the peak position to higher energy for these two samples, with the magnitude of the shift being greater for sample G. (The seemingly large peak shift in sample E is an unfortunate artifact of barrier Al content. This sample was grown at a different

time in the MBE system cycle, whereas the other samples were grown consecutively). Previous studies on quantum wells grown on LTGaAs buffer layers have shown similar trends in peak shift to higher energy [6]. In that case, it was suggested that the presence of increasing strain due to higher concentration of excess As in the buffer layers was responsible for the observed energy shift. For the present growth structures, strain is an unlikely explanation. The LTGaAs layers are very thin and it has been shown that annealing at T_{ab}>580°C for 10 mins. is sufficient to remove the lattice mismatch to GaAs even for bulk layers of LTGaAs [4]. In this case, annealing at 600°C removes the source of the peak broadening mechanism. Both annealed samples, D and E, exhibit linewidths comparable to the control sample (10 meV). However, the effect of non-radiative traps remains significant in E, which contains no AlAs barriers. Nonetheless, this effect is reduced by the anneal.

In the case of the 150Å well, whose position in the growth means that it always sees unannealed LTGaAs, the effects are different. Again the optical efficiency of the well decreases compared to the control sample, with sample G having lowest efficiency. However, now sample F exhibits the highest intensity emission, comparable to the control. Interestingly, the linewidth is fairly uniform for all four samples (5 meV), indicating there is no induced interface disorder associated with backdiffusion from the LTGaAs layer. The decreased efficiency of the two annealed samples is probably due largely to the long anneal in an As_4 overpressure, rather than the LTGaAs.

We believe that there is a simple explanation for these results based on point defect considerations. When GaAs is grown at low temperatures, excess As is incorporated in the cystal implying a high concentration of As-rich related native defects, i.e. V_{Ga},As_{Int} and As_{Ga} type defects. Only the latter has been positively identified in LTGaAs [4], and then only for unannealed samples. As-related complexes are also likely to exist, to account for the remainder of the 1 at.% excess As. The thin LTGaAs layers in our growth structures are consequently highly localized sources of these defects in non-equilibrium concentrations..

As the lattice temperature is raised these native defects become more energetic and they will attempt to re-establish equilibrium concentrations. To do so, they must move through the crystal. Defect diffusion in III-V heterostructures has been extensively studied (readers are referred to review article by Deppe and Holonyak [8]). The observed broadening of the 50Å peak strongly suggests that the group III sublattice is involved in the forward diffusion defect migration mechanism. Therefore, we propose the following simple defect reaction as a possible first step in the redistribution mechanism for excess As in LTGaAs:

$$As_{Ga} \rightarrow V_{Ga} + As_{Int}$$

As the temperature increases many defect pairs of this type are created, with the reaction being driven by the highly non-equilibrium conditions. Typically the group III vacancy (V_{III}) defects have the highest diffusion rates of the six

possible native defects in III-V crystals. The V_{Ga} defects therefore can out-diffuse from the LT layer due to the concentration gradient much faster than the As_{int} defects. These vacancies will preferentially diffuse in the direction of the growth surface which is under an As_4 overpressure, since they can decrease the free energy of the crystal by self-annihilation at the surface. As they move forward through the crystal predominantly by hopping to adjacent group III sublattice sites they induce interface intermixing of group III atoms. The average Al content of the well increases (from zero) and that of the barrier material will decrease as the V_{III} moves across the GaAs/AlGaAs interface.This will inhomogeneously shift the 2D energy levels higher. This explains the broadening of the 50Å QW PL peak and its observed shift to higher energy in the unannealed samples. The ability to prevent such an effect may be of great importance in structures that are sensitive to interface-scattering or alloy-scattering effects. There is a relatively small effect due to vacancy outdiffusion observed in samples D and E because the anneal takes place immediately following the LTGaAs layer. The growth surface is therefore less than 40 lattice sites from the V_{Ga} defects which consequently find it easily. By the time the 50Å well is deposited, the native defect concentration of this type of defect is already at its equilibrium value.

AlAs layers were initially used as diffusion barriers because of the higher Al-As bond strength compared to Ga-As bonding. Since an Al atom must break its As bonds for the vacancy to propagate through AlAs, the V_{III} diffusion rate will be much lower in AlAs than in GaAs. Although sample F demonstrates that the 30Å AlAs barriers in our structures are not completely effective at preventing vacancy outdiffusion, they do offer a significant improvement over no barriers (sample G). Nevertheless, 30Å is a very thin layer, and thicker diffusion barriers can be expected to fully protect the integrity of epilayers grown on LTGaAs.

The 150Å well is not affected by V_{Ga}-induced intermixing since it is away from the preferential diffusion direction. The PL for this well does not display significant broadening effects. However, both wells display the effects of non-radiative recombination sites, which can be attributed to As_{int} defects and related complexes. As the temperature increases, their tendency is also to reduce the local non-equilibrium concentration. In this case the diffusion path involves hopping between neighboring interstitial sites or through some intermediate configuration involving mostly group V sublattice sites. Consequently we do not expect this type of defect motion to have a large effect on group III atomic positions. However, these defects do affect the optical efficiency of quantum wells when they are present by providing carrier trap centres. From our studies it is not clear which, if any, is the preferential diffusion direction for the As_{int} type defects, although simple thermodynamics arguments suggest that backdiffusion would dominate for a sample in an As_4 overpressure. Indeed, the 150Å well data shows the PL quenching effect most clearly. In samples F and G we see that the insertion of AlAs barriers is definitely effective at inhibiting defect backdiffusion when we compare their optical efficiency.

Summary

We have studied the optical properties of thin layers of LTGaAs using PL measurements. Quantum wells containing even a few monolayers of material grown at 230°C were found to be optically dead which suggests the defects associated with LT growth are very effective at quenching radiative recombination. Outdiffusion and backdiffusion of these defects was investigated by their effect on nearby QW's. Group III atom intermixing effects is observed in the direction of the growth surface, which suggests that V_{Ga} defects due to the LTGaAs are involved in the defect migration mechanism. The insertion of AlAs barriers was found to significantly reduce the defect diffusion problem, being most effective against backdiffusion. Annealing the sample immediately following the LTGaAs improved outdiffusion effects by allowing defects to anneal out.

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The Role of Microstructure in the Electrical Properties of GaAs Grown at Low Temperature

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We have examined the role of As precipitates on transport through undoped GaAs grown at low temperature by molecular beam epitaxy and annealed at high temperature. Temperature dependent I-V measurements exhibit two regimes. At temperatures less than ~200K, transport attributed to point defect-associated hopping conduction is observed even for samples annealed at 750°C. For temperatures greater than ~200K, the transport is quantitatively consistent with calculations of thermally assisted tunneling emission of electrons from metallic As precipitates acting as buried Schottky barriers.

Key words: High field, precipitates, transport, tunneling emission

INTRODUCTION

The material characteristics of low-temperature-grown (LTG)-GaAs have been studied by various groups due to its potential applications as a semi-insulating epitaxial layer.[1] The growth of GaAs at ~200°C by molecular beam epitaxy (MBE) is highly non-stoichiometric with ~1–2% excess arsenic being incorporated in solid solution during growth.[2] Following high temperature anneals (~600°C), the excess arsenic forms precipitates embedded in the GaAs matrix.[3] Among other interesting properties, the annealed material is found to be highly resistive. In one model, the high resistivity is qualitatively explained by viewing arsenic precipitates as buried Schottky barriers with overlapping depletion regions.[4] The metallic nature of the precipitates is supported by recent scanning tunneling microscopy results.[5] For such a model, the transport properties should quantitatively reflect the observed microstructural features. By combining the temperature dependence of I-V data with microstructure data obtained by transmission electron microscopy (TEM), we show that high field transport in annealed LTG-GaAs is consistent with thermally assisted tunneling of electrons from metallic As precipitates. A simple one-dimensional calculation is found to agree well with the experimental data.

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DISCUSSION

To study transport at high fields, an n^+/LTG-i/n^+ structure was used, as shown in Fig. 1. The n^+ GaAs layers were degenerately doped with Si at a level of 2×10^{18} cm^{-3}. Following growth of the n^+ buffer at 600°C, a thin 5×(5Å AlAs/10Å GaAs) superlattice was grown to inhibit outdiffusion of the excess arsenic in the LTG layer during annealing.[6] Growth was then interrupted while the substrate temperature was ramped to 230°C, followed by growth of 5000Å of LTG-GaAs. The substrate temperature was then ramped

to 450°C and a top cladding superlattice and the n^+ cap were deposited. This growth architecture was employed to minimize spatial variations in the precipitate distribution. The sample was cleaved and annealed separately in a rapid thermal annealer for 30s at 600, 650, 700, and 750°C. A mesa structure diode was fabricated, with alloyed AuGe/Ni/Au contacts.

At room temperature, the observed transport properties of the LTG-GaAs layer are similar for all annealing temperatures (T_{anneal}). However, the temperature dependence measurements reveal more complex behavior, in which the transport is sensitive to the annealing temperature and the measurement temperature. For the sake of clarity, our results are summarized in schematic form in Fig. 2. We find evidence for two transport mechanisms. At low temperatures (<200K) the temperature dependence of the I-V data is attributed to defect-associated hopping conduction. This behavior has previously been shown to dominate the low-field transport in unannealed LTG-GaAs.[7] This result suggests that there is a significant residual concentration of point defects in the LTG-GaAs layer that has not precipitated out of solution even for annealing temperatures as high as 750°C. Indeed, for the sample annealed at 600°C, hopping conduction dominates the transport for nearly all measurement temperatures. Figure 3a shows the temperature dependence for samples annealed at different temperatures. As expected, we observe that the hopping conduction contribution to transport decreases as T_{anneal} increases, consistent with continued precipitation of As-related point defects.

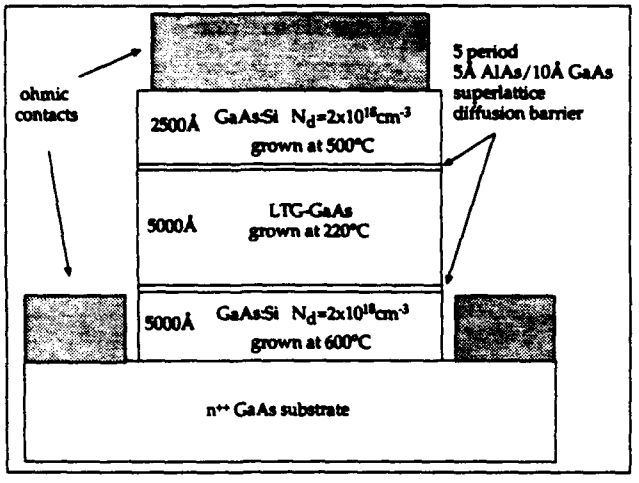


Fig. 1. Schematic of growth architecture used to study transport through LTG-GaAs annealed at different temperatures.

Except for the sample annealed at 600°C, transport at temperatures >200K is clearly dominated by a mechanism other than hopping conduction. In this regime, the transport exhibits a strong temperature dependence, with an activation energy of ~0.6 eV. In Fig. 3b, we show the I-V data at various T>200K for the sample annealed at 700°C. The current exhibits an approximately exponential dependence on the voltage, suggesting transport over a potential barrier. Since the contribution from point defects is decreased, we take the buried Schottky barrier model as a starting point in order to explain the high field transport properties for temperatures greater than ~200K.

Assuming that the precipitates are metallic, then we can model LTG-GaAs as a series of N equivalent metal/semiconductor/metal (MSM) junctions, where N is the total thickness of the LTG-GaAs layer multiplied by the average number of precipitates per unit length. Each junction is essentially a pair of back-to-back Schottky diodes, and we need only consider the transport through one MSM junction, since the electric field is the same across the LTG-GaAs layer. The average junction width can be measured directly by TEM. For the sample annealed at 700°C, TEM analysis yielded a precipitate density of 1.7×10^{16} cm^{-3}, and an average precipitate diameter of 107Å, from which

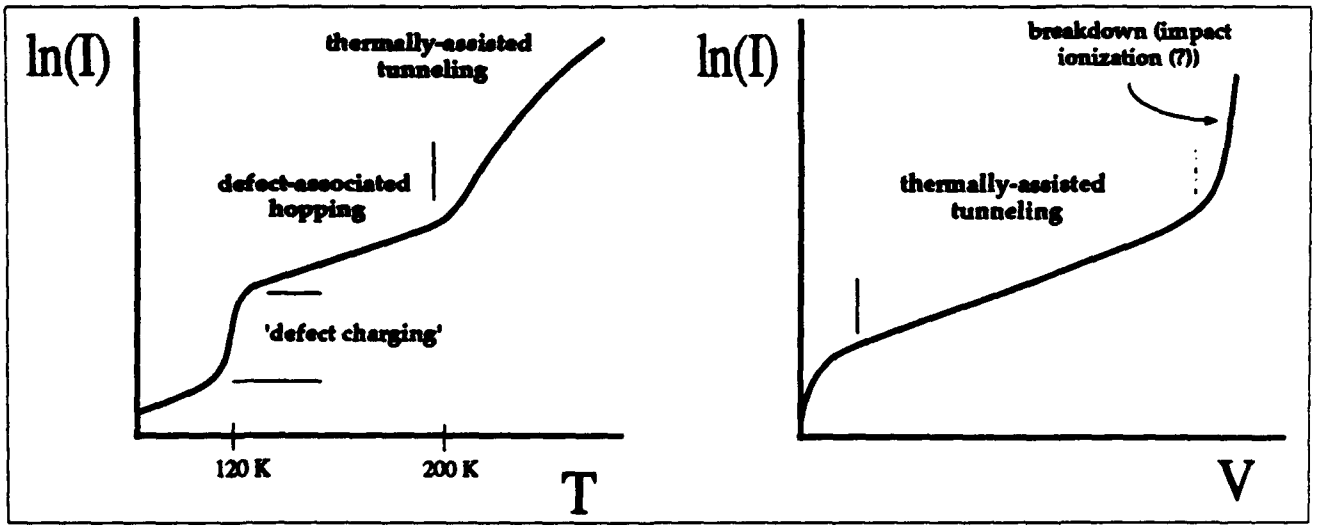
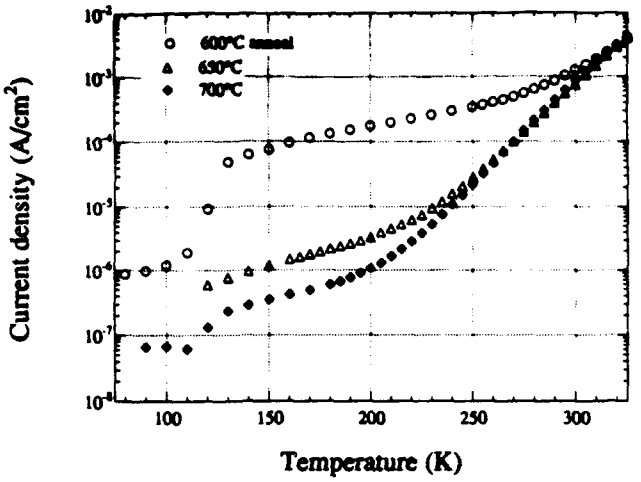


Fig. 2. Schematic summarizing data obtained from I-V measurements as a function of temperature. Behavior attributed to hopping conduction associated with point defects is observed in all samples at lower temperatures. The high temperature (>200K) behavior is consistent with tunneling emission from metallic As precipitates.



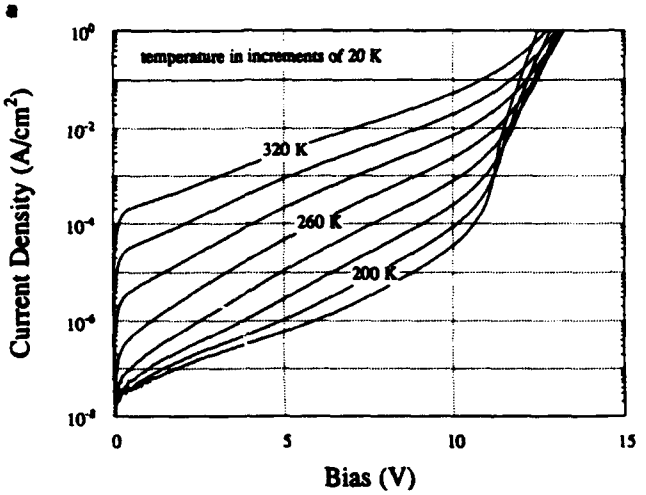


Fig. 3. (a) Current measured at 5 V bias as a function of temperature for samples annealed at 600, 650, and 700°C. As the annealing temperature increases, the contribution due to hopping conduction decreases. (b) Current-voltage measurements taken at various temperatures (200–320K) for the sample annealed at 700°C. For T > 200K, hopping conduction is negligible and the current is exponentially dependent on the applied bias.

an average junction width of 285Å was obtained. Since even a relatively high residual doping of 1×10^{18} cm^{-3} results in a maximum band-bending between Schottky barriers of only ~0.1 eV, it is reasonable to neglect free carrier conduction in the material between precipitates.

The equation for current flow due to thermionic emission over a reverse-biased Schottky barrier is given by the Richardson equation, modified to include image-force barrier lowering effects due to an applied electric field, ε. This gives a current equation with a $\varepsilon^{1/2}$ dependence. In our case, we also have to include a geometric factor, g, due to the finite size of the precipitates. An approximate value can be obtained from TEM results, by multiplying the mean precipitate cross-section area with the mean areal density. For this sample, a factor of 0.06 is obtained. A comparison between the calculated thermionic emission current density as a function of junction electric field, and the

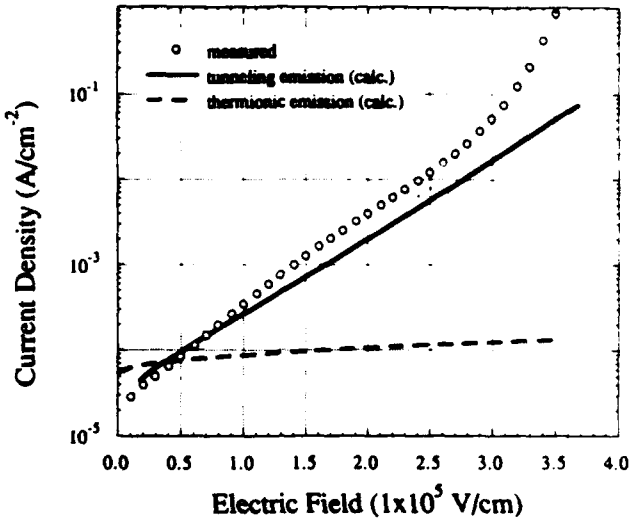


Fig. 4. Measured current-field dependence compared with calculations of thermionic emission, and tunneling emission current flow from metallic As precipitates. A Schottky barrier height of 0.6 eV was used in the calculations.

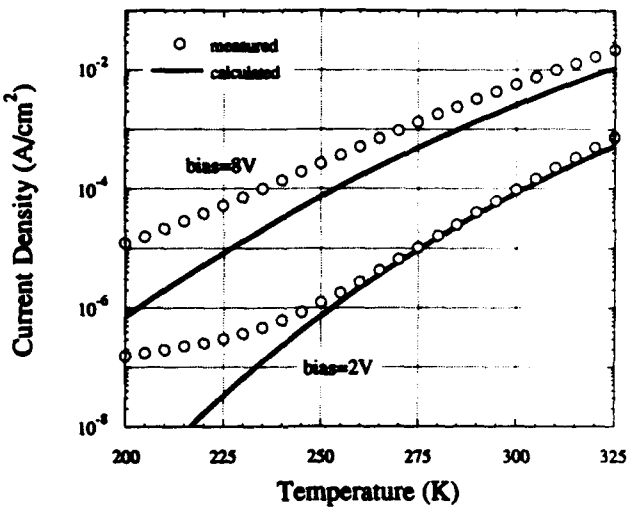


Fig. 5. Measured current-temperature dependence compared with calculations of tunneling emission current flow from metallic As precipitates.

measured data are shown in Fig. 4, using a barrier height of 0.60 eV. We find that the calculated current density gives the correct magnitude at low fields. However, thermionic emission theory does not correctly predict the field dependence.

Reconsidering the MSM band diagram and noting that the electric fields in the junction are large (~1×10^5 V/cm), we calculated the current through the reverse biased Schottky barrier taking into account both thermionic emission over the barrier and tunneling emission below the barrier tip. The expression for the total current density is given by[8]

$$J = \frac{qmkT}{2\pi h^3} \int_0^\infty \exp\left(-\frac{E}{kT}\right) P(E,\varepsilon)\,dE$$

where $P(E, \varepsilon)$ is transmission probability for an electron with energy E. $P(E, \varepsilon)$ explicitly contains the field

dependence since the potential energy profile of the barrier changes with the applied field. Since the Wentzel-Kramers-Brillouin method is not valid for electron energies near the top of the potential barrier, we employed a numerical method based on transmission matrices to calculate P(E, ε). This method discretizes the potential energy profile into a large number of potential steps. Complete details of the calculation will be discussed elsewhere.[9] Figure 4 shows the calculated and experimentally obtained current as a function of the junction field at 300K, for a barrier height of 0.6 eV. We find that there is good agreement between our model and the experimental data. The temperature dependence of the current, which arrives from the Fermi distribution of carriers in the precipitates, is shown in Fig. 5. Again, the calculated dependence is in good agreement with the experimental data.

CONCLUSION

In conclusion, we have studied the high field transport through undoped LTG-GaAs annealed at different temperatures above 600°C. Arsenic precipitates are present in all samples, but the transport temperature dependence suggests a significant background level of point defects have not precipitated out of solution. The background level, as qualitatively determined from the sample conductivity, decreases with increasing annealing temperature. By correlating microstructural features in samples annealed at temperatures greater than 650°C, the high temperature (>200K) transport is found to be quantitatively consistent with calculations of thermally assisted tunneling emission of electrons from metallic precipitates acting as buried Schottky barriers. The calculated electron transport through LTG-GaAs using a simple one dimensional model agrees well with both the observed field-dependence and the observed temperature-dependence.

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Temperature Investigation of the Gate-Drain Diode of Power GaAs MESFET with Low-Temperature-Grown (Al)GaAs Passivation

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We have investigated the breakdown-temperature characteristics of the gate-drain diode of a GaAs metal semiconductor field-effect transistor with low-temperature-grown (LTG) GaAs/AlGaAs passivation. An anomalous decrease in the breakdown voltage as a function of the temperature is observed. This behavior leads us to propose an explanation of how LTG passivation leads to a high breakdown voltage at room temperature; and this explanation in turn allows us to predict the power performance of the passivated devices.

Key words: Breakdown, LT-GaAs, MESFET, passivation

INTRODUCTION

The product of the maximum drain current and the gate-drain breakdown voltage is a good indication of the microwave power performance of a device. Whereas arbitrary value of drain current can be obtained by simply changing the channel epitaxial layer, a design that leads to a high gate-drain breakdown voltage is much more elusive. Recent works which incorporated the low-temperature-grown (LTG) GaAs as a surface passivant along with an overlapping gate structure have demonstrated dramatic improvement in the gate-drain breakdown voltage.[1,2] However, the mechanism through which the LTG passivating layer improves the breakdown voltage is not completely understood. In this work, we have fabricated and studied the temperature dependence of the gate-drain diode of a GaAs metal semiconductor field-effect transistor (MESFET) with LTG-(AlGaAs/GaAs) passivation and an overlapping gate structure. We have observed an anomalous decrease of the breakdown voltage at low temperature. By investigating this behavior, we can qualitatively explain how an LTG-passivant improves the gate-drain breakdown voltage.

(Received April 12, 1993)

DEVICE FABRICATION

The epitaxial structure was grown by molecular beam epitaxy (MBE) (Varian 360) on a (001) semi-insulating GaAs substrate. First, a smoothing buffer layer of 5000Å GaAs was grown at a substrate temperature of 600°C, followed by 1860Å of n-GaAs, and an arsenic-diffusion-barrier of 200Å of AlAs.[3] The substrate temperature was then lowered to 200°C, and 1000Å of LTG-GaAs was grown, followed by 1500Å of LTG-$Al_{0.3}Ga_{0.7}As$. The mobility and sheet charge concentration were determined from van der Pauw measurements on a separate structure, to be 3700 $cm^2/V\text{-}s$ and 3.8×10^{12} cm^{-2}, respectively.

The fabrication process of the device began with the definition of the mesa by wet chemical etching of the patterned sample. Next, the source-drain regions were defined and reactive-ion-etching (RIE) with Cl_2 was used to remove the insulating layers and expose the channel.

AuGe/Ni/Au ohmic contacts were defined by lift-off

and subsequent rapid-thermal-annealing at 375°C for 15 s resulting in a contact resistance of 0.3 Ω-mm. The foot of the gate was then defined and again RIE with Cl_2 was used to etch away the LTG layers down to the channel. Finally, the overlapping gate mask was aligned to the defined gate foot print and the gate was then formed by lift-off of Ti/Au metals. The schematic representation of the final cross-section profile of the device is shown in Fig. 1.

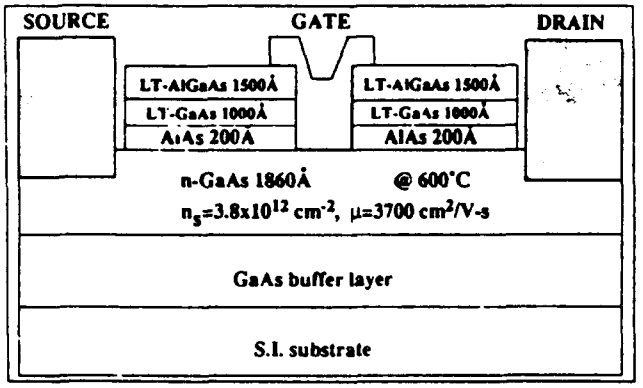

Fig. 1. Schematic representation of the cross section profile of a GaAs MESFET with LTG-($Al_{0.3}Ga_{0.7}As$/GaAs) passivation and overlapping gate structure.

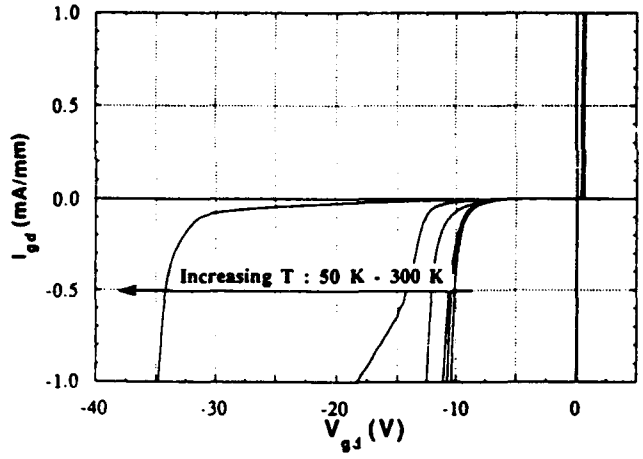

Fig. 2. Gate-drain diode characteristics at different temperature of a LTG-($Al_{0.3}Ga_{0.7}As$/GaAs) n-GaAs MESFET.

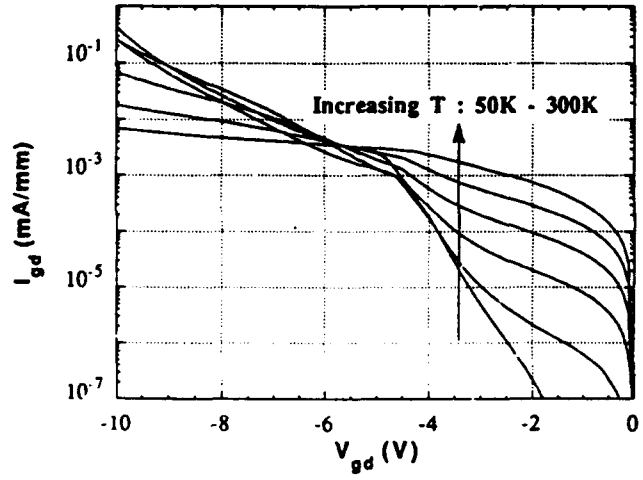

Fig. 3. Semi-log plot of the gate-drain diode characteristics.

RESULTS

The temperature characteristics of the gate-drain diode of a 1.2 μm gate-length GaAs MESFET with LTG-AlGaAs/GaAs passivation is shown in Fig. 2. At 300K, the diode shows a high breakdown voltage of 34 V. However, as the temperature is lowered, the breakdown voltage first decreased monotonically, then saturated to about 10 V at 7 K. A semi-log plot of the diode characteristic is shown in Fig. 3. In comparison, Fig. 4 shows the temperature-dependence behavior of a gate-drain diode in a conventional GaAs MESFET ($N_d = 3 \times 10^{17}$ cm^{-3}). In the conventional device, the observed dependence of the breakdown voltage with temperature is very small.

On-wafer continuous-wave power measurement of 1.2 μm × 300 μm devices are performed at 4 GHz. The output power and power-added-efficiency at a bias of V_{ds} = 13 V and V_{gs} = −1.5 V are shown in Fig. 5. The maximum power density obtained is 820 mW/mm at 26.4 % PAE.

DISCUSSION

The strong temperature dependence of the breakdown voltage observed in a MESFET with LTG-GaAs passivation can be explained by using existing breakdown models.[4,5] In the low gate voltage range, the current-voltage characteristics shown in Fig. 3 agree with the transport model of thermionically assisted tunneling between precipitates proposed by Ibbetson et al.[6] The electrons propagate from the gate metal onto the LTG-GaAs passivation layer by tunneling via the assistance of the local electric field and the temperature. However, since the electric field drops off rapidly away from the gate metal, the injected electrons are localized at those precipitates that are close to the gate metal. The resulting excess of the negative charges in the vicinity of the gate metal next

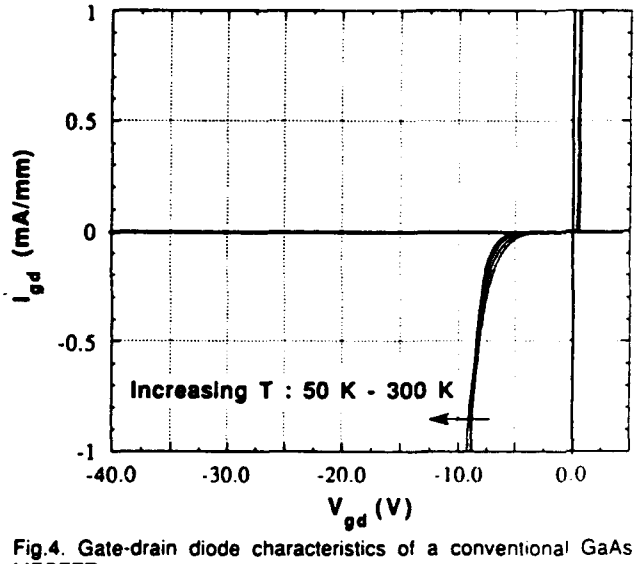

Fig.4. Gate-drain diode characteristics of a conventional GaAs MESFET.

to the drain would redistribute the associated electric field. Consequently, the peak electric field at the edge of the gate is alleviated. As the temperature is lowered, the number of electrons that can thermionically field emit into the precipitates is significantly reduced, thus the LTG-GaAs becomes less effective in reducing the field. At low temperature (77K), this field alleviation mechanism becomes relatively ineffective; thus, the breakdown voltage saturates at that of a conventional GaAs MESFET. Figure 6 shows schematically the electric field distribution with the field alleviation by the charged precipitates. The most conservative hypothesis we can draw is that, since the response of traps at low temperature is similar to their high frequency response, the rf breakdown may be close to the breakdown voltage at 77K. Even so, a large benefit results as explained below.

To obtain the maximum output power from MESFETs, the devices are usually biased at half of the breakdown voltage thereby allowing the rf signal to swing from zero to the rf breakdown voltage (BV_{rf}). However, the static electric field at the gate edge for LTG-passivated devices is low even at a gate-drain bias as high as BV_{rf} ($BV_{rf} << BV_{dc}$). We, therefore, expect that a full rf swing of $2 \times BV_{rf}$ can be accomodated in these devices, doubling (at the minimum) the rf power from passivated devices compared to conventional GaAs MESFETs. The power measurements on our device shown in Fig. 5 supports the above hypothesis.

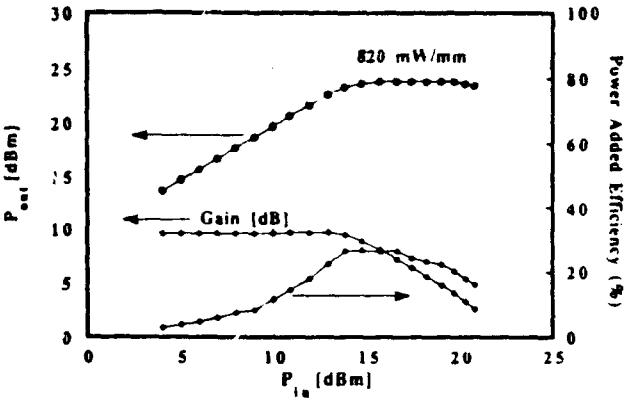

Fig. 5. Output power and power-added efficiency vs input power at 4 GHz for a 1.2 × 300 μm device.

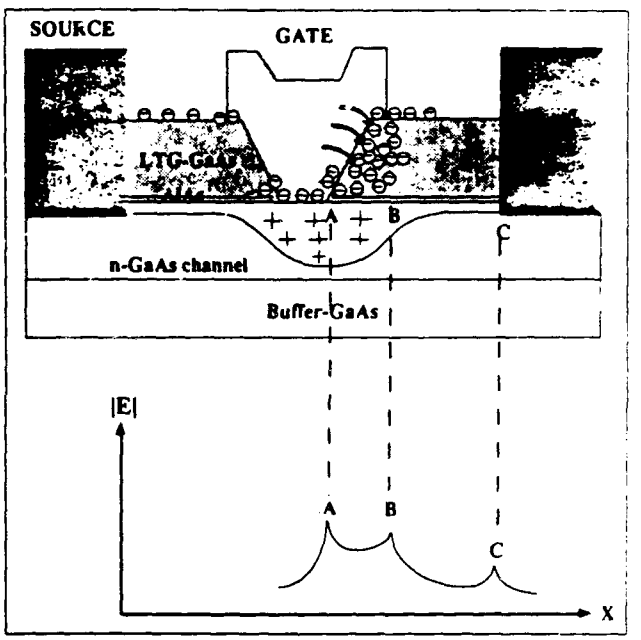

Fig. 6. Field redistribution by trapped charges at the gate metal edge at 300K.

CONCLUSION

By experimentally investigating the temperature dependence of the current-voltage characteristics of the gate-drain diode, we were able to explain the role that an LTG-($Al_{0.3}Ga_{0.7}As$/GaAs) layer plays in the alleviation of the electric field at the drain edge of the gate metal. This alleviation of electric field leads to a much higher breakdown voltage compared to that of the conventional MESFET. The device was able to deliver 820 mW/mm at 26.4 % PAE @ 4 GHz.

ACKNOWLEDGMENT

The authors would like to thank Wei-Nan Jiang for his assistance in the temperature measurement of the devices. This work is supported by the U.S. Air Force Office of Scientific Research (AFOSR-91-0111) and Hewlett Packard (MICRO); U.K. Mishra is supported by an NSF PYI Award (ECS-9144723).

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DEVICE PERFORMANCE OF SUBMICROMETRE MESFETs WITH LTG PASSIVATION

L.-W. Yin, N. X. Nguyen, K. Kiziloglu, J. P. Ibbetson, A. C. Gossard and U. K. Mishra

Indexing terms: MESFETs, Passivation

The device characteristics of a submicrometre GaAs MESFET with low-temperature-grown GaAs passivation are reported. The fabricated device has a high gate-drain breakdown voltage of over 20 V with a maxium drain current of 340 mA/mm and a transconductance of 200 mS/mm. Microwave measurement of the device yields a cutoff frequency of 32 GHz, and an unusually high maximum frequency of oscillation of 110 GHz. These combined characteristics demonstrate the potential of the device as a viable power amplifier in the millimetre-wave frequency range.

Introduction: The recent advent of the technology of passivation with low-temperature-grown (LTG) GaAs and related materials has dramatically improved the power performance of GaAs based field effect transistors [1, 2]. For long gate length (1 μm) devices, LTG-GaAs passivation has repeatedly led to the improvement of the gate–drain breakdown voltage without the sacrifice of either the maximum drain current or the transconductance; this combination of DC device characteristics has resulted in the observed improvement in the maximum power density of the device [3]. In this work, we have fabricated a submicrometre device with LTG-GaAs passivation; this device also showed a dramatic improvement in the gate–drain breakdown voltage with high cutoff frequency.

Device design and fabrication: The epitaxial structure was grown by a Varian Gen II MBE system on semi-insulating LEC GaAs substrate. First, a smoothing buffer layer of 5000 Å undoped GaAs was grown at a substrate temperature of 600°C, then 1000 Å of *n*-channel GaAs, followed by an arsenic-diffusion barrier of 200 Å of AlAs. The substrate temperature was then lowered to 220°C, where 1000 Å of LTG-GaAs was grown; the sample was annealed *in-situ* by raising the substrate temperature to 600°C for 10 min. The mobility and sheet charge concentration were determined from the Van der Pauw measurement to be 3020 cm^2/Vs and $5{\cdot}13 \times 10^{12}\,cm^{-2}$, respectively.

The fabrication process of the device began with the definition of the mesa by wet chemical etching of the patterned reactive-ion etching (RIE) with Cl_2 was used to remove the LTG-GaAs layer and expose the channel. AuGe/Ni/Au ohmic contacts were evaporated and lifted off. Subsequently the contacts were alloyed by rapid-thermal annealing at 375°C. The contact resistance of the device is ~0·3 Ω mm. Next, the submicrometre gate was defined using e-beam lithography, and the LTG-GaAs in the gate area was again removed using Cl_2 RIE. The overlapping gate was then written on top of the gate area by an e-beam writer. Finally, the Schottky gate of Ti/Au metals was deposited and lifted off. The resulting cross-section profile of the finished device is shown schematically in Fig. 1.

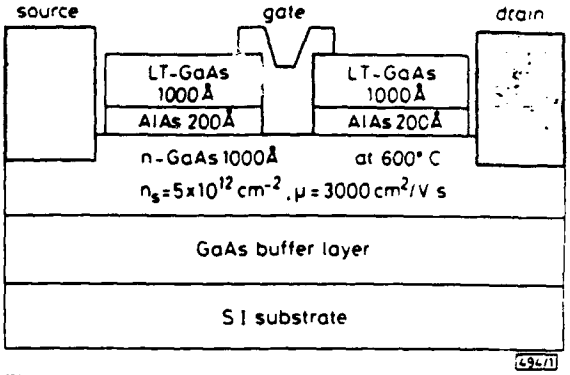

Fig. 1 *Schematic representation of cross-section profiles of finished device*

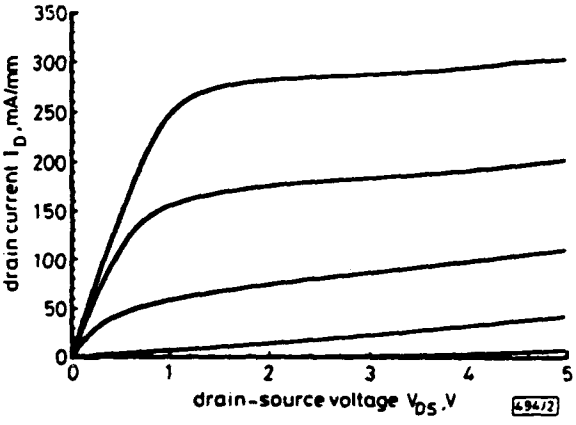

Fig. 2 *Drain current-voltage characteristics*
V_g (start) = 0·5 V, V_g (step) = −0·5 V, V_g (stop) = −2 V

Results and discussion: The device has a metallurgical gate length of 0·3 μm, with an overlapping gate metal of 0·3 μm. The gate is centred between the source to drain spacing of 3 μm (Fig. 1). DC measurement of the device characteristics was performed using an HP-4145B parameter analyser. The nominal current–voltage output characteristics of a device are shown in Fig. 2. Across a 1 × 1 cm^2 sample, the transconductance of the devices varies from 200 to 230 mS/mm, with the maximum drain current ranging from 290 to 340 mA/mm. The gate–drain breakdown voltage BV_{gd} of the devices, defined at the reverse leakage current of 1 mA/mm, varies from 25 to 18 V. These breakdown voltages are about twice those of conventional GaAs MESFETs with comparable gate lengths. Again, this improvement in the breakdown voltage is attributed to the field alleviation by the excess stored charges in the LTG passivation layer [2]. A summary of the figures of merit of the devices is shown in Table 1. The observed uniformity of the device characteristics reasserts the potential of LTG passivation as a viable technology for millimetre-wave power devices.

Table 1 SUMMARY OF FIGURES OF MERIT OF MESFET WITH 0·3/0·5 μm OVERLAPPING GATE LENGTHS

L_g	I_{max}	I_{dss}	g_m	V_{GD}	f_T	f_{max}
μm	mA/mm	mA/mm	mS mm	V	GHz	GHz
0·3/0·5	290–340	188–227	196–234	18–25	28–32	90–110

quency range 40 MHz–40 GHz using an HP-8510B automatic network analyser. Electrical contacts were made using a pair of Tektronix coplanar probes. The measured current gain cutoff frequency f_T varies from 28 to 32 GHz. Linear extrapolation of the unilateral gain curve yields a maximum oscillation frequency f_{max} of 90–110 GHz. The ratio of f_T to f_{max} is unusually high for conventional devices with similar peripherals; we believe that this is a consequence of the LTG passivation, but further studies are needed to quantify this effect. Measurement of f_T as a function of the drain to source voltage V_{DS} shows a clear dispersive relationship between the cutoff frequency and the applied bias (Fig. 3). This reduction in the cutoff frequency at high V_{DS} is due to the lateral extension of the drain depletion region [4].

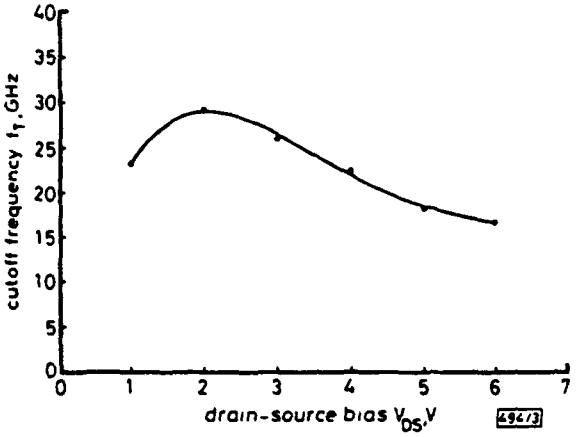

Fig. 3 *Cutoff frequency as function of drain-source biases*

Conclusion: LTG passivation is demonstrated to be an attractive technology for GaAs MESFET in millimetre-wave power applications. The measured DC characteristics of the devices promise high power performance. The unusually high f_{max} observed in the device is attributed to the LTG passivation layer, however further investigations are needed to understand this effect. Typical dispersion of the current gain cutoff frequency as a function of the source to drain voltage is also observed.

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23rd June 1993

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ENCAPSULATED GaAs POWER MESFET

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ABSTRACT

Utilizing a combination of Low-Temperature-Grown $Al_{0.3}Ga_{0.7}As$ passivation, overlapping gate, MOCVD regrown of the source/drain contacts, and isolation by boron ion implantation, we have fabricated a GaAs MESFET with completely encapsulated channel. Electrical characterization of the device shows that the early catastrophic on-state breakdown is suppressed. In contrast to the usually observed characteristics in GaAs MESFET, the breakdown locus of the device also has a positive slope. These improvements should allow us to bias the device at a higher operating point, thereby increasing the obtainable maximum output power in the device.

I. INTRODUCTION

The surface of the device has been recognized as a major source of many detrimental effects on the performance of GaAs MESFET. Various theoretical studies over the years have led to the conclusion that the surface played a significant role in the device characteristics[1-3]. In particular, the breakdown voltage and instability in the current-voltage family of curves are two surface related parameters that directly effect the power performance of a device. In recent years, the surface of the device in the vicinity of the gate has been indirectly addressed by the advent of the low-temperature-grown (LTG) passivation and overlapping-gate technology [4],[5]. Devices which utilized these technology have demonstrated dramatic improvement in the gate-drain breakdown voltage, which in turn drastically enhanced the power output by the devices [4-6]. However, little attention has been paid to the exposed surfaces near the source and drain regions. In this work, we have attempted to address this issue by developing a technology to fabricate MESFETs with an encapsulated channel; and from the study of these fabricated devices, we have gained a better understanding in the role of the surface in GaAs MESFETs.

II. DEVICE DESIGN AND FABRICATION

Figure 1 shows a schematic representation of the epitaxial structure of the samples used in this experiment. All the samples were grown by a Varian Gen II MBE system on

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semi-insulating LEC GaAs substrate. Standard growith procedure started with a smoothing buffer layer of 5000 Å of undoped GaAs grown at 600 °C, followed by the channel; then an arsenic-diffusion-barrier of 200 Å of AlAs. The substrate temperature was then lowered to 200 °C, where 2000 Å of LTG-$Al_{0.3}Ga_{0.7}As$ was grown. The samples were then annealed in-situ at 600 °C for 10 minutes.

Preparation for selective regrowth of the source/drain regions began with a blanket deposition of 1500 Å of SiO_2 by PECVD at 250 °C. The samples were then patterned with a source/drain mask by photolithography. The SiO_2 in the open areas were removed using reactive ion etching with plasma CF_4; followed by a selective wet etching of the LTG-$Al_{0.3}Ga_{0.7}As$ by citric acid. Then the AlAs was etched in diluted HF, and finally citric acid was used to etch about 300 Å into the GaAs channel layer. n++ GaAs was regrown in the open areas using MOCVD at 550 °C. After the MOCVD regrowth of the source/drain regions, the samples were patterned for isolation by multiple boron ion implantation. Subsequent standard processing steps to define the ohmic and gate metals have been reported elsewhere [6].

III. RESULT AND DISCUSSION

Figure 2 shows the characteristics of a device without complete encapsulation of the channel, the device has a gate-drain breakdown voltage of about 29 V. However, as shown in the drain current-voltage family of curves, the device has a catastrophic breakdown at V_{DS} = 17.5 V and V_{GS} = 0.5 V; therefore this is an inherent limitation of the voltage swing of the device for power performance. Continuous wave on-wafer measurement of the power of the device at 4 GHz is shown in Figure 3; the device delivered 620 mW/mm with a power-added-efficiency of 30 %.

In comparison, the preliminary device characteristics of a GaAs MESFET with an encapsulated channel is shown in Figure 4. Although the gate-drain breakdown voltage of this device is only 11 V; we were able to bias the device up to V_{DS} = 7 V and V_{GS} = -2 V for power measurement. From the drain current-voltage characteristics, we also observed that the device breakdown locus shows a definite positive slope. The device outputs 520 mW/mm with a PAE of 18 % at 4 GHz (Figure 6). Although the maximum output power of this device is lower than that of the above device, the limitation is due to the lower gate-drain breakdown voltage not the catastrophic breakdown. Therefore, we believed that we should be able to improve the power performance of the device by just improving the gate-drain breakdown voltage.

On another sample with higher gate-drain breakdown voltage (20 V), Figure 5; we again noticed that the catastrophic on-state breakdown is suppressed. The device also displays a positive slope of the breakdown locus. The regrowth contact resistance obtained from the TLM measurement is 0.7-0.8 Ω-mm. However, it should be noted that this quoted resistance included the resistance of the regrown layer along with the interfacial resistance.

IV. SUMMARY

We have proposed a technology for the fabrication of a GaAs MESFET with a completely encapsulated channel. Electrical characterization of these devices show that the catastrophic on-state breakdown voltage is suppressed, and the breakdown locus of the devices displays a positive slope. These DC characteristics allow the device to be biased at a higher operating point, thereby increasing the power obtainable from the device.

ACKNOWLEDGMENT

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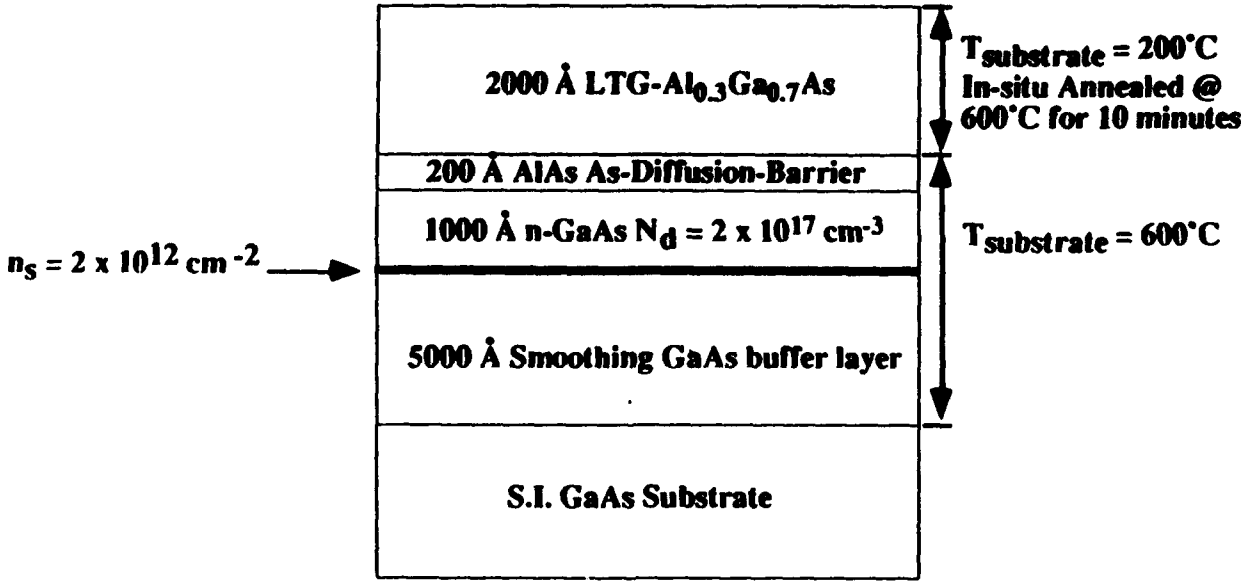

Figure 1 : MBE epitaxial structure and growth conditions

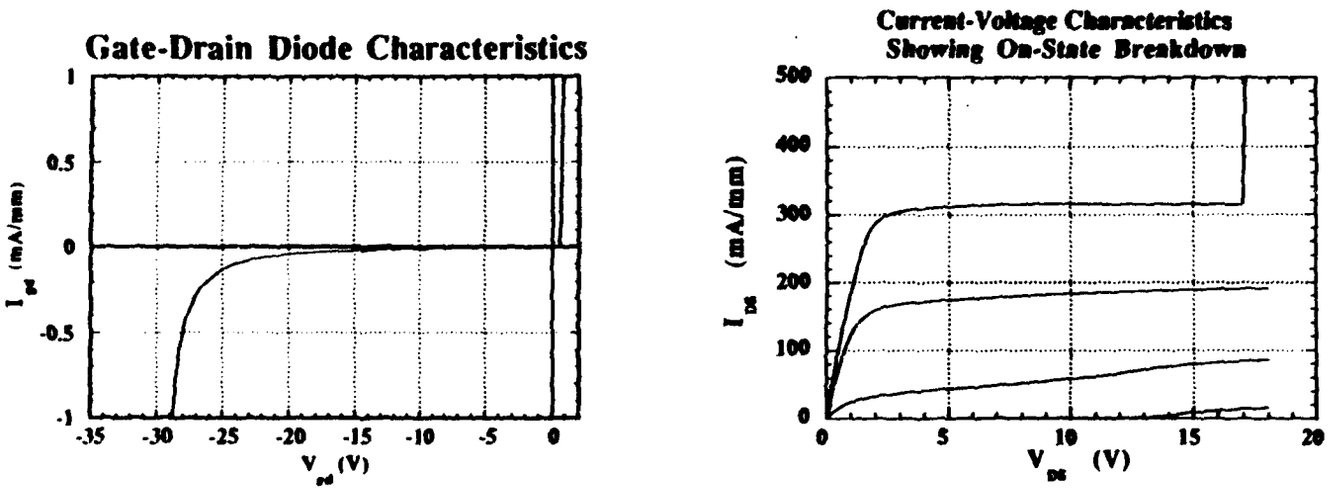

Figure 2 : DC characteristics of the device without complete encapsulation of the channel

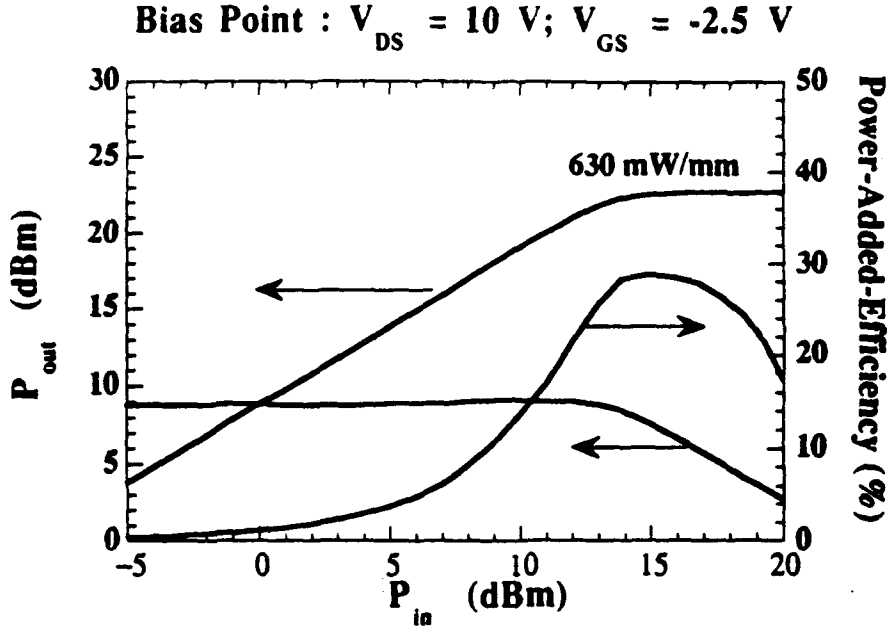

Figure 3 : Power performance of a GaAs MESFET without complete encapsulation of the channel at 4 GHz

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Figure 4 : DC characteristics of preliminary GaAs MESFETs with encapsulated channel

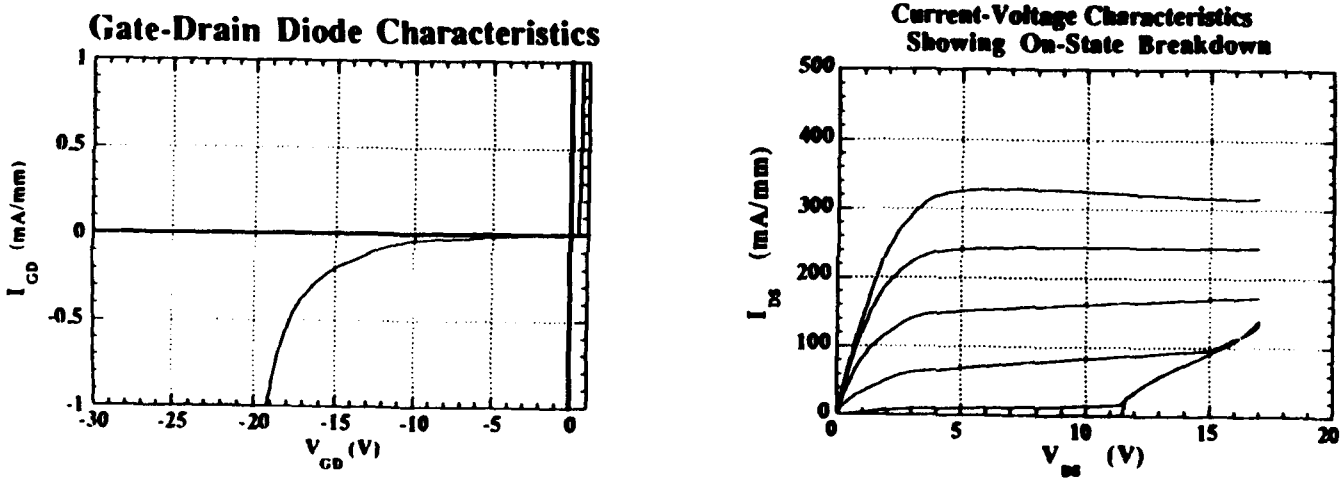

Figure 5 : Device characteristics of a GaAs MESSFET with an encapulated channel and high gate-drain breakdown

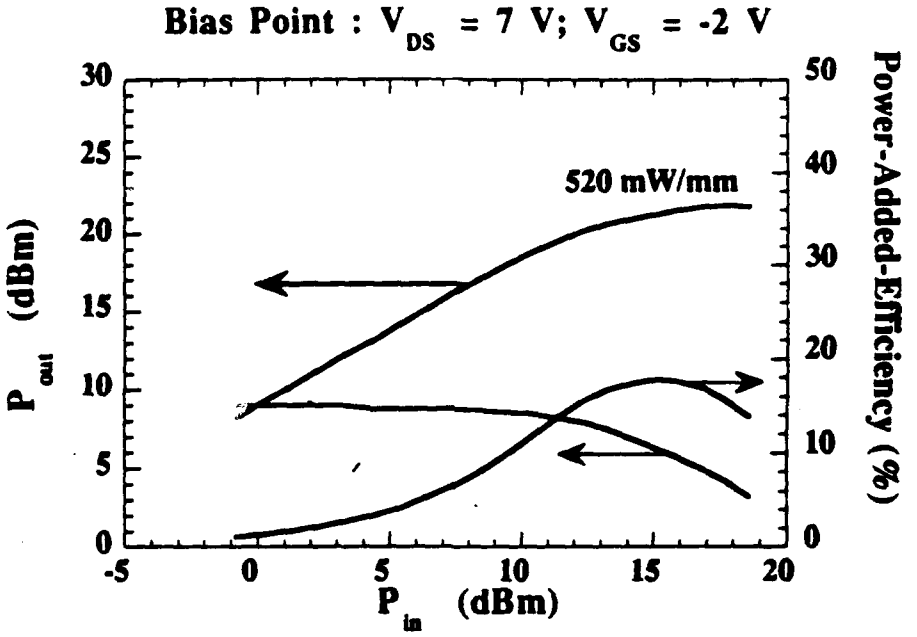

Figure 6 : Power performance of an encapsulated channel GaAs MESFET at 4 GHz